

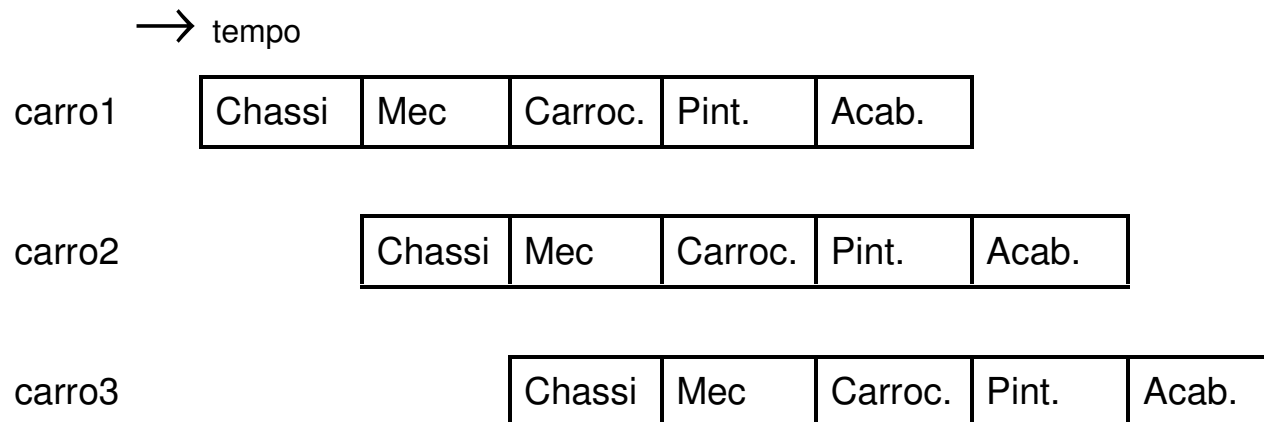
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# **Chapter Six**

## **Pipelining**

# Pipelining: analogia com linha de produção

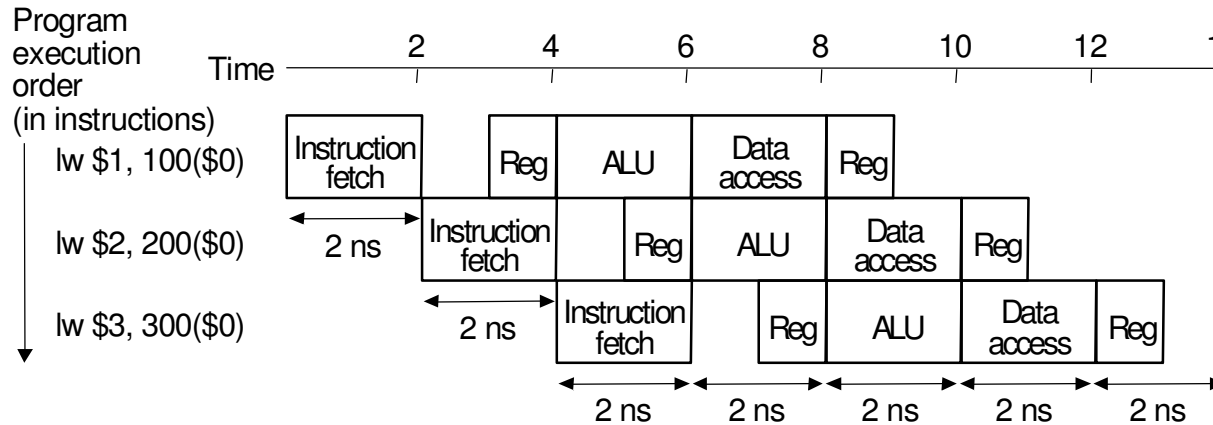
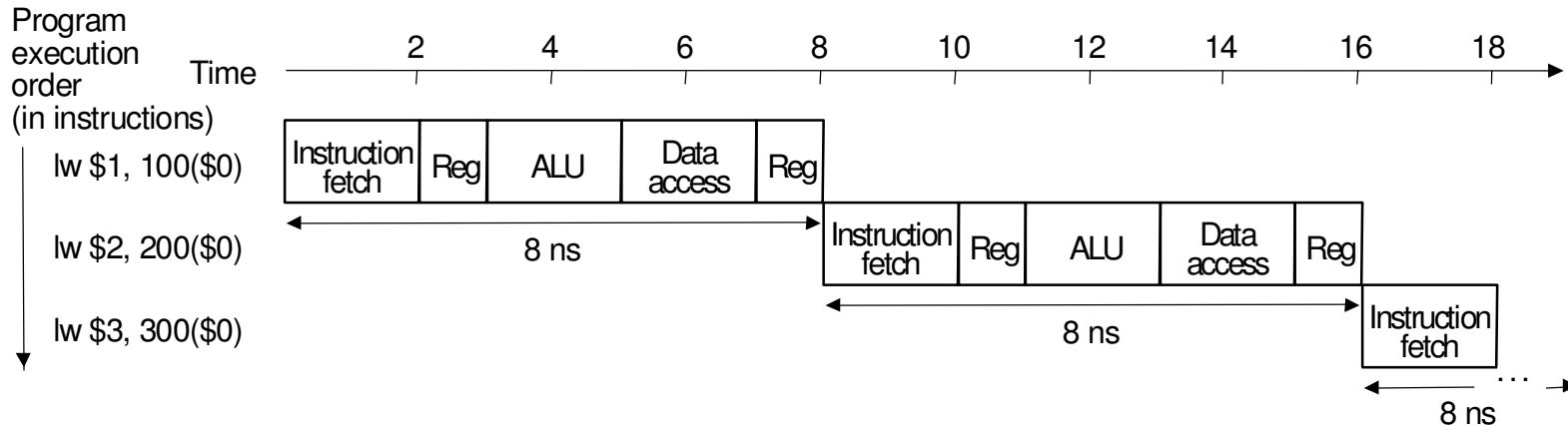
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- **Tempo de fabricação de um carro:  $C+M+C+P+A$**
- **Taxa de produção (carros/h): medido na saída**
  - **throughput: depende do número de estágios e do balanceamento**
- **Objetivo do pipeline:**
  - **distribuir e balancear o tempo em cada estágio**
  - **otimizar o uso de HW dos estágios (taxa de ocupação)**
  - **resumo: aumentar a velocidade e diminuir o hardware**

# Pipelining

- Improve performance by increasing instruction throughput



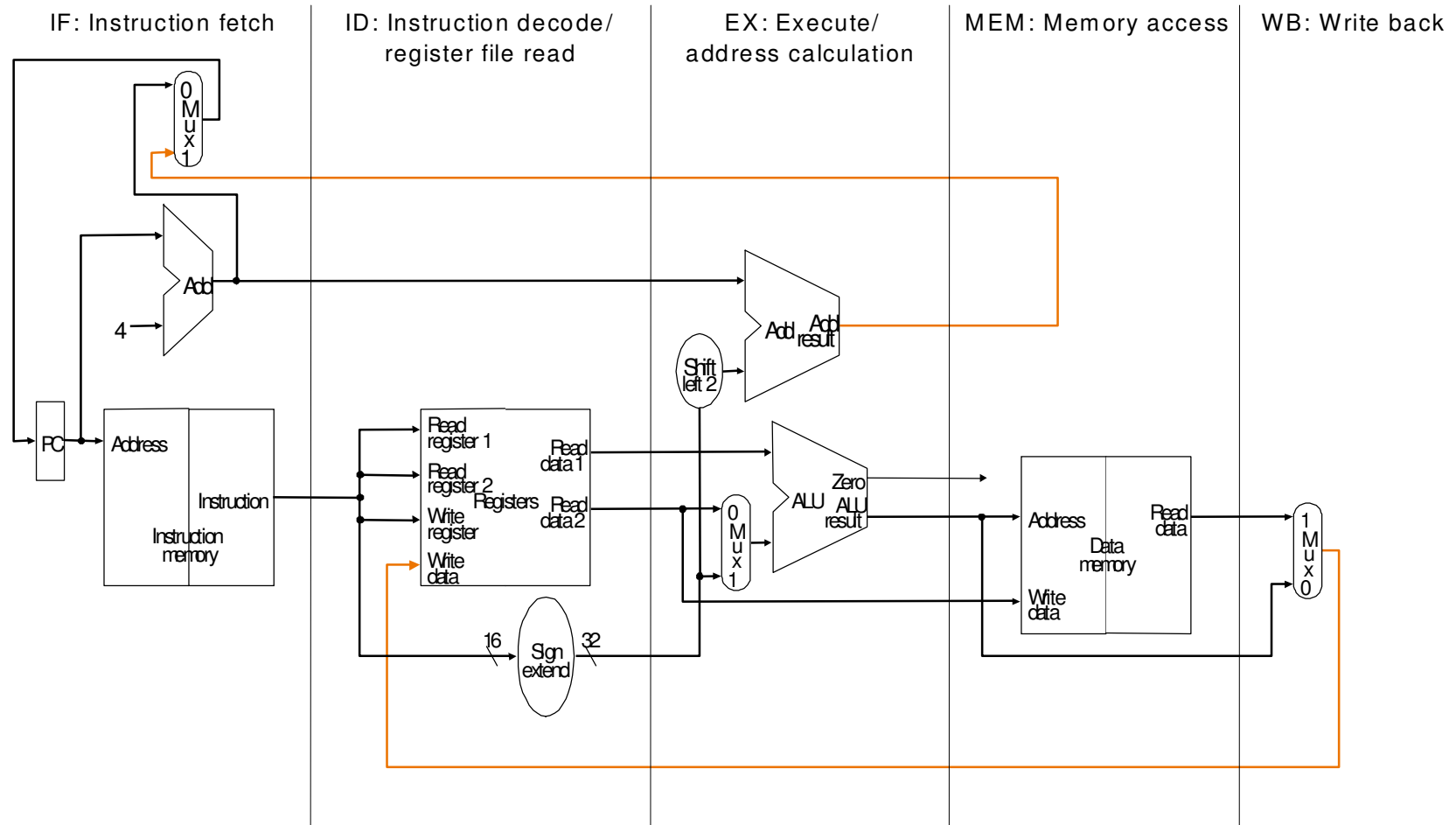
- tempo de execução de uma instrução: 8 ns e 9 ns (com ou sem pipe)
- throughput: 1 instr / 8ns (sem pipeline) ou 1 instr / 2 ns (com)
- # de estágios = 5; ganho de 4:1; para obter 5:1 ??

# Pipelining

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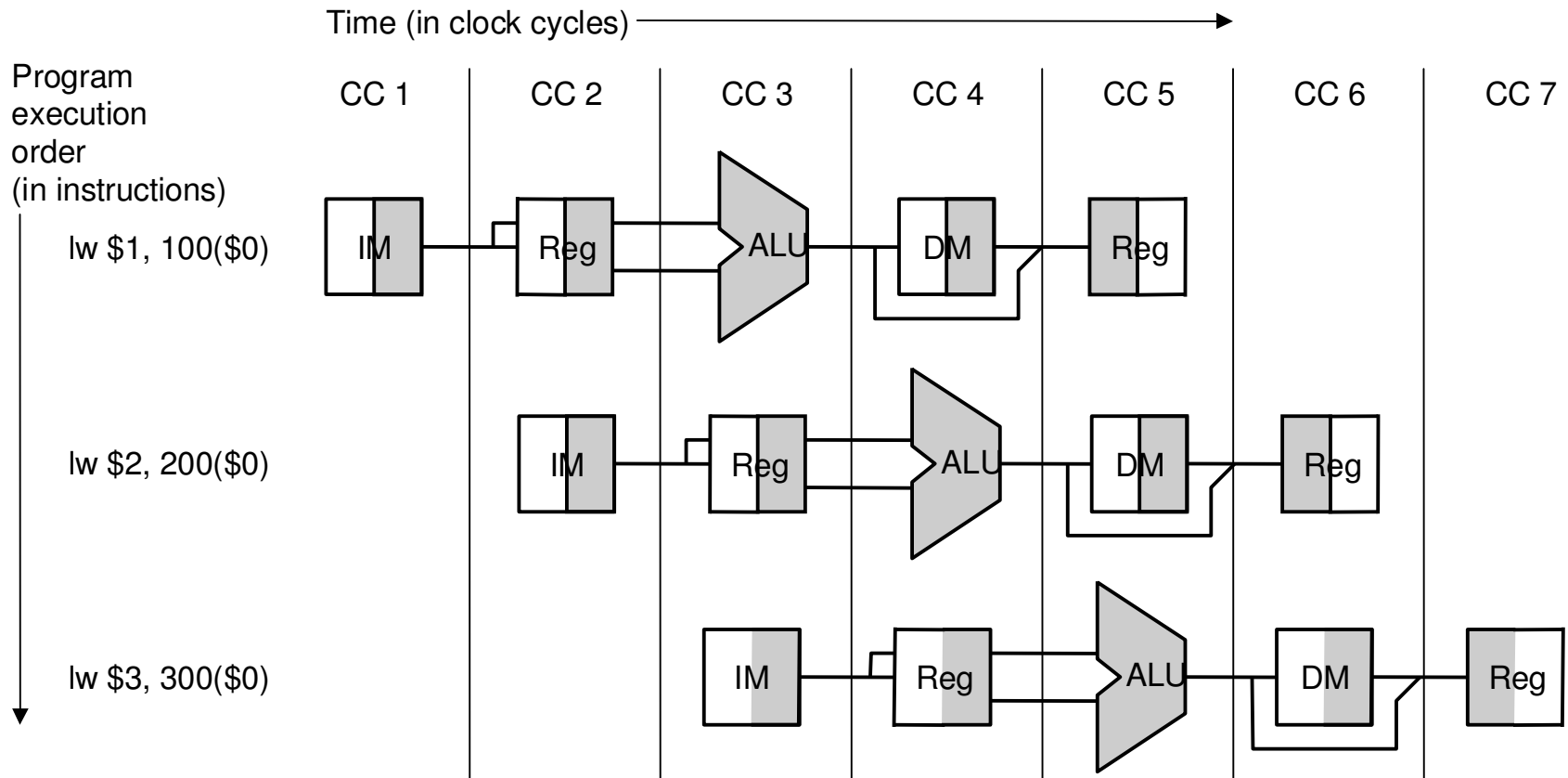
- **What makes it easy**
  - all instructions are the same length
  - just a few instruction formats
  - memory operands appear only in loads and stores
- **What makes it hard?**
  - structural hazards: suppose we had only one memory
  - control hazards: need to worry about branch instructions
  - data hazards: an instruction depends on a previous instruction
- **We'll build a simple pipeline and look at these issues**
- **We'll talk about modern processors and what really makes it hard:**
  - exception handling
  - trying to improve performance with out-of-order execution, etc.

# Basic Idea



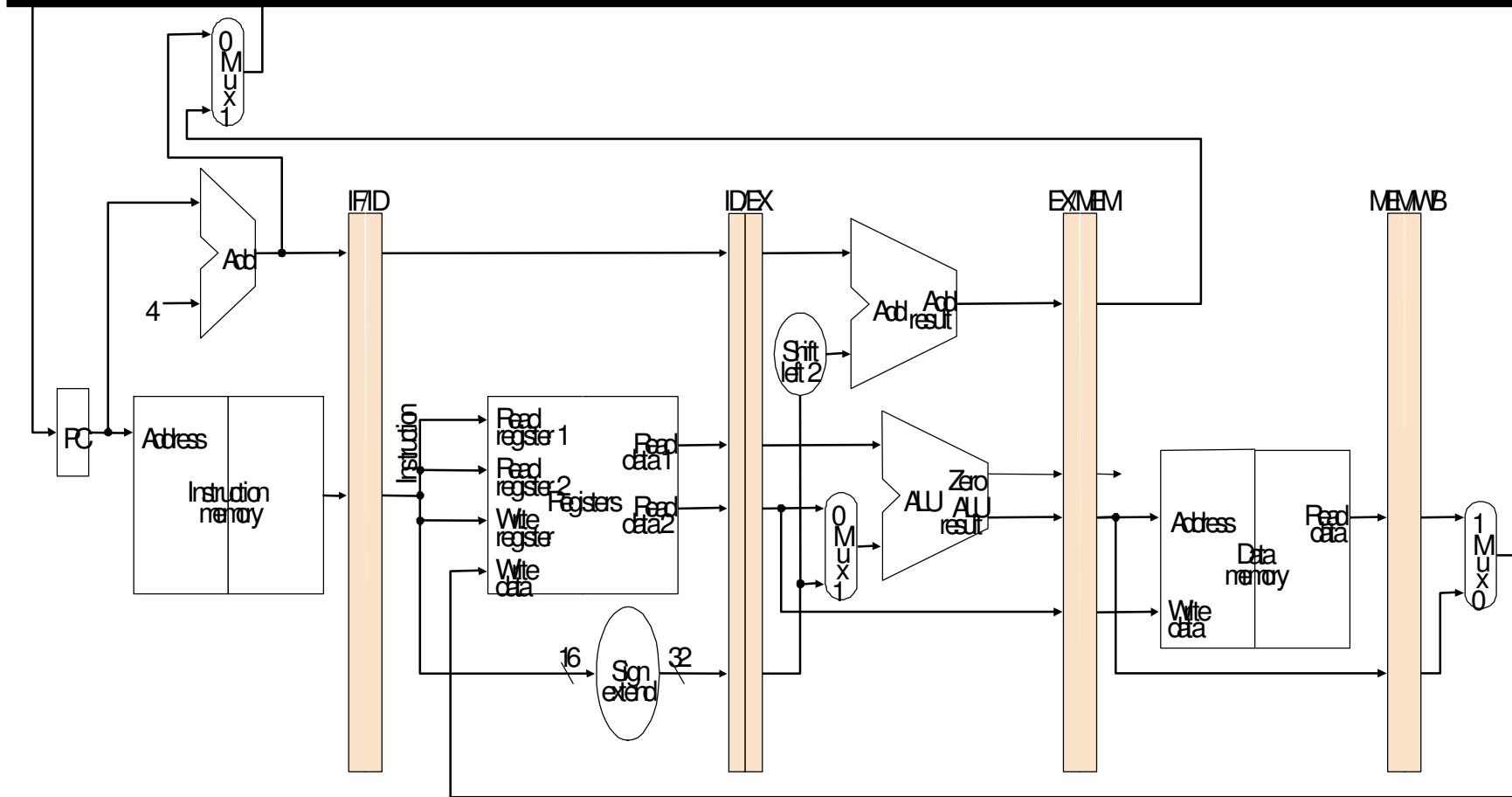
- *What do we need to add to actually split the datapath into stages?*

# Uma representação para o pipeline



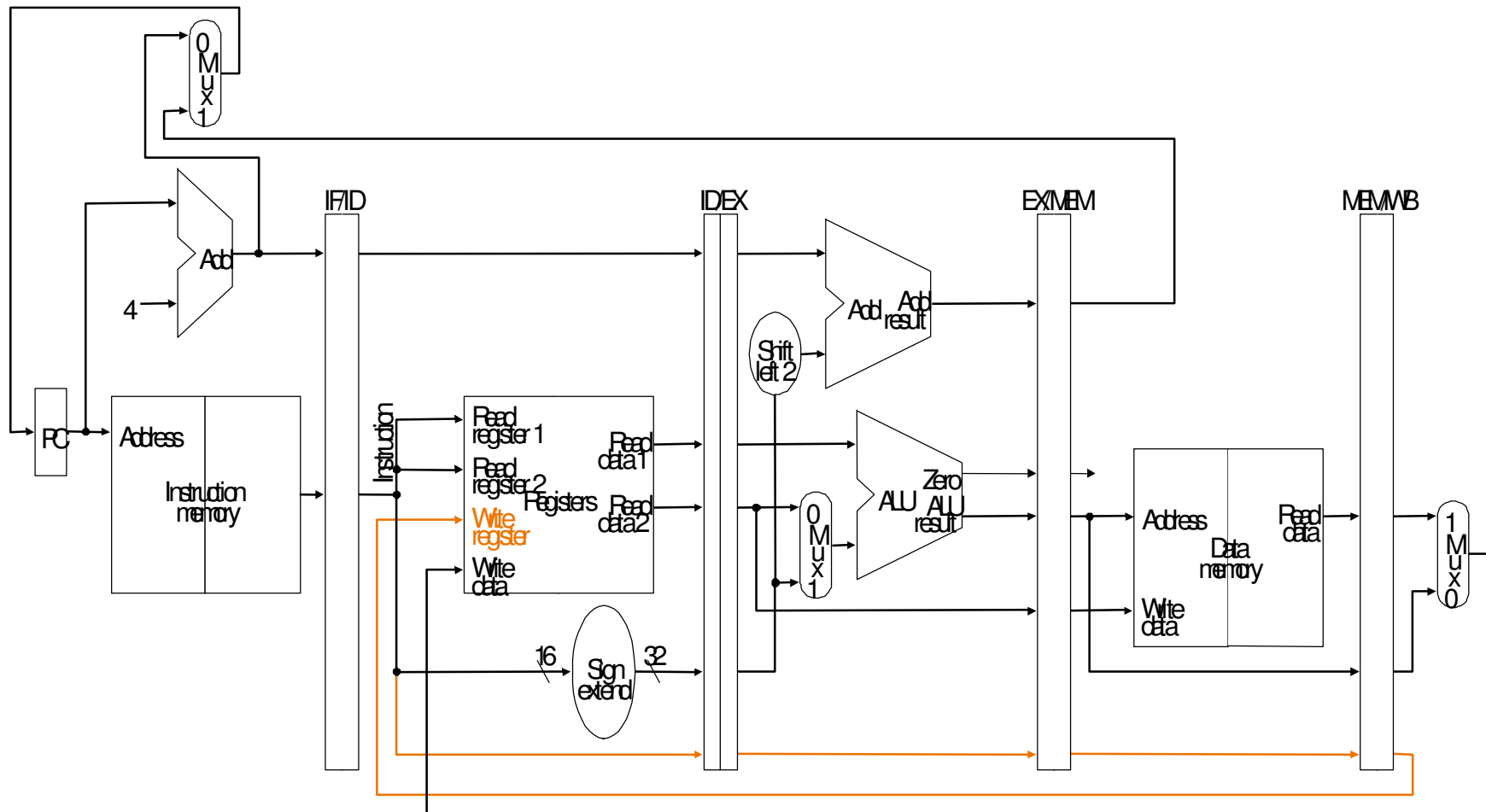
- **Hachurado representa “atividade”**
- **Representação alternativa: imaginando que cada instrução tenha a sua própria via de dados**
- **Outra representação: foto no tempo**

# Pipelined Datapath



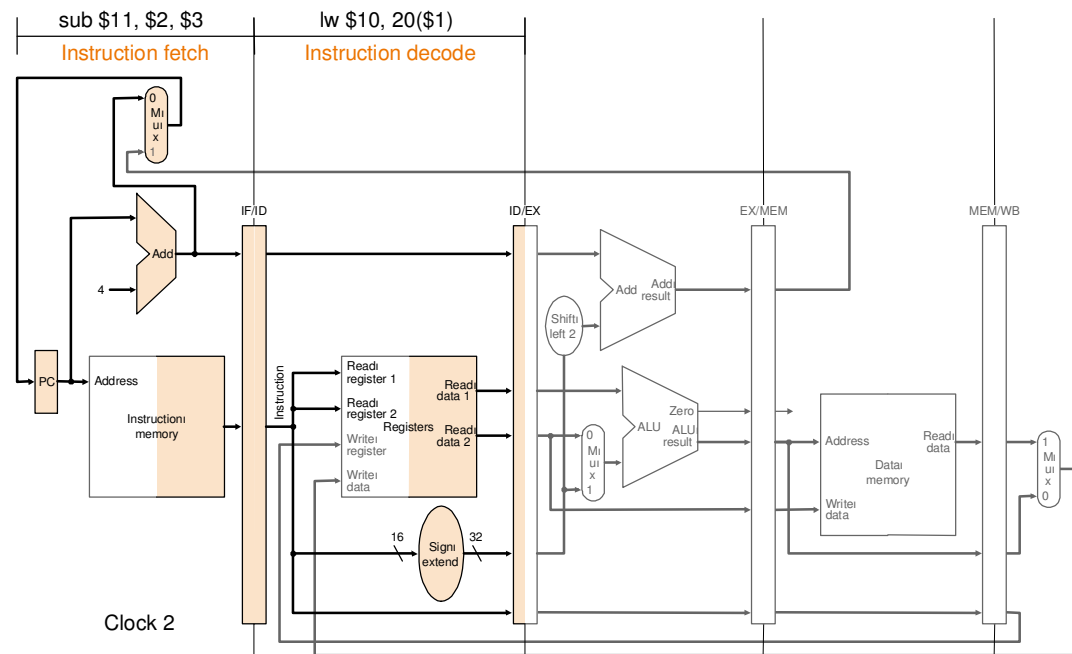
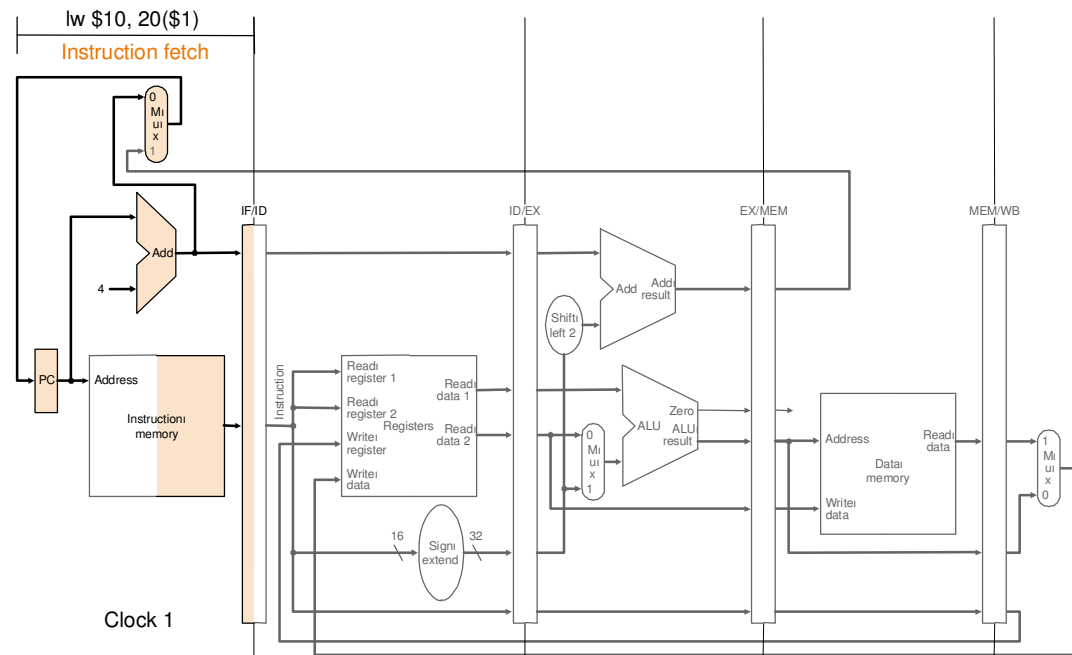
- O que é produzido em cada estágio é armazenado em um registrador de pipeline para uso pelo próximo estágio
- Problemas com o endereço do registrador de escrita?? Caminhando para esquerda?

# Corrected Datapath

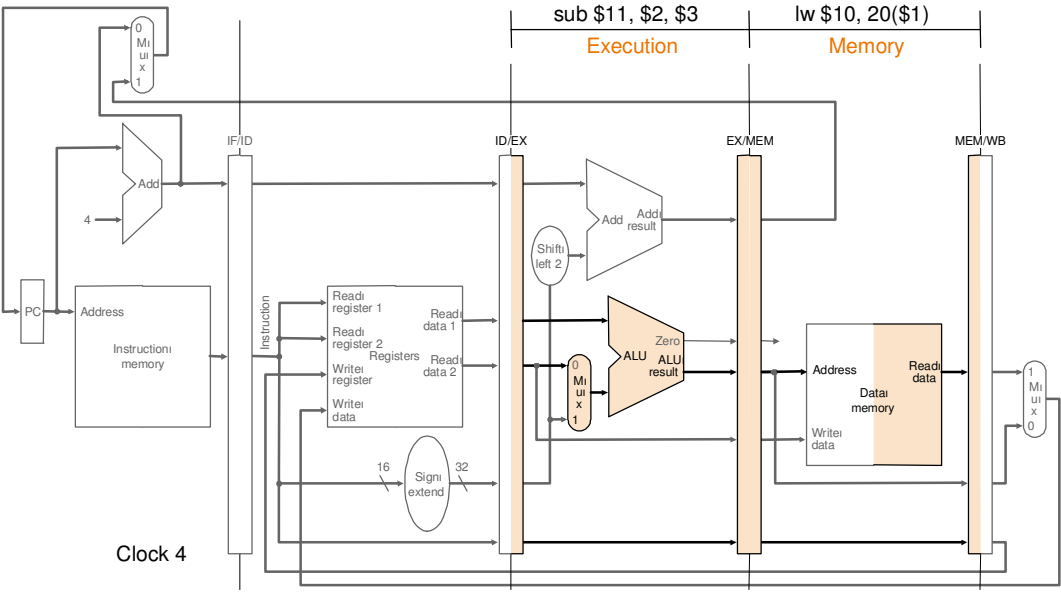
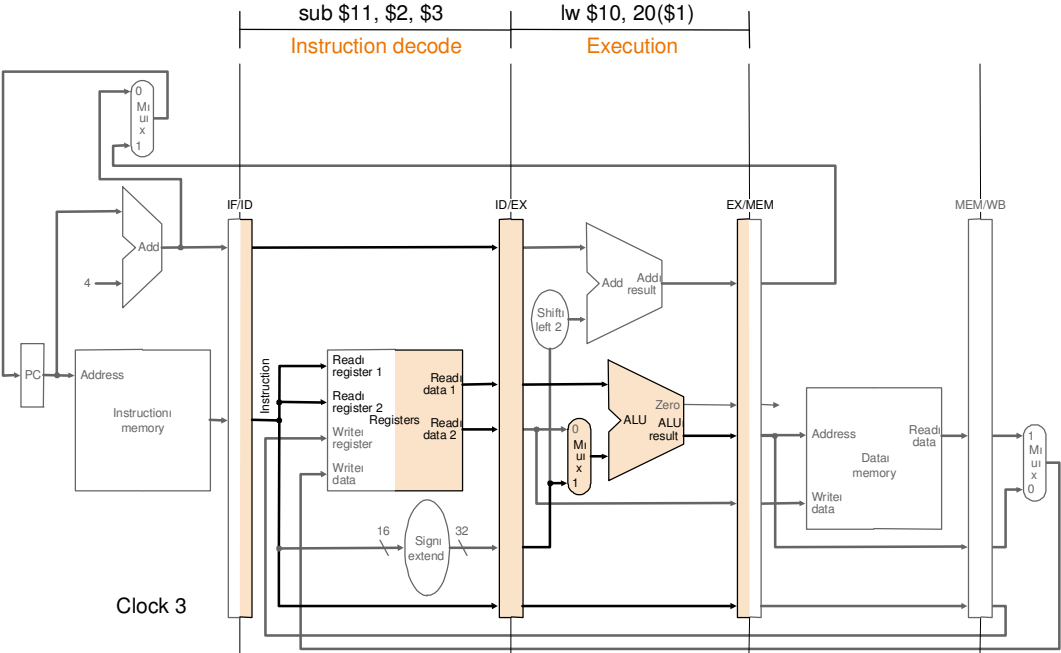




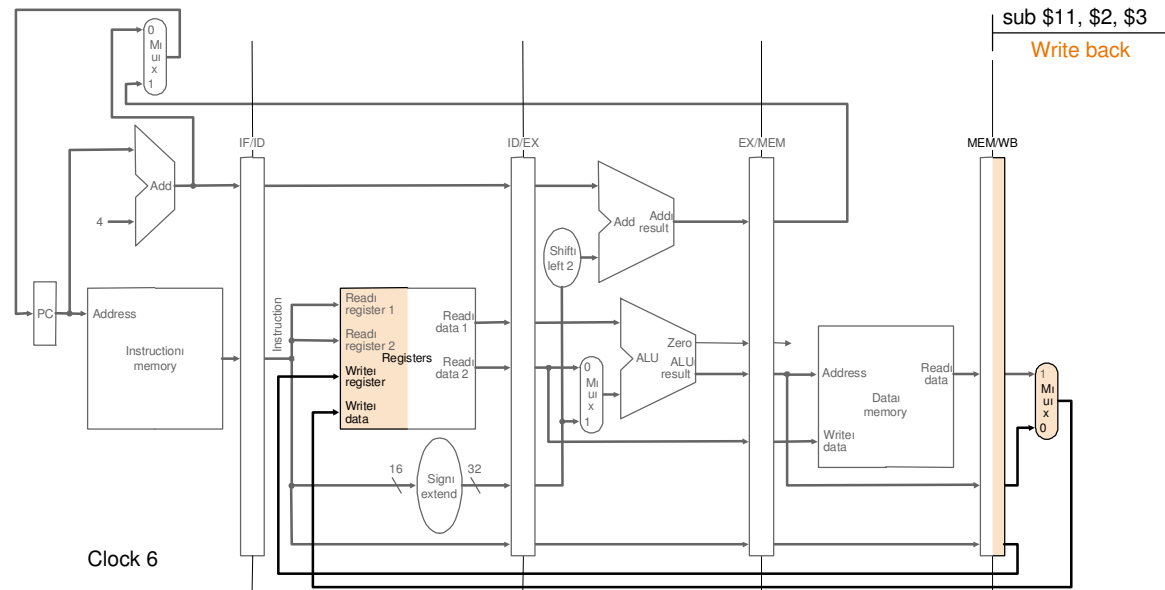
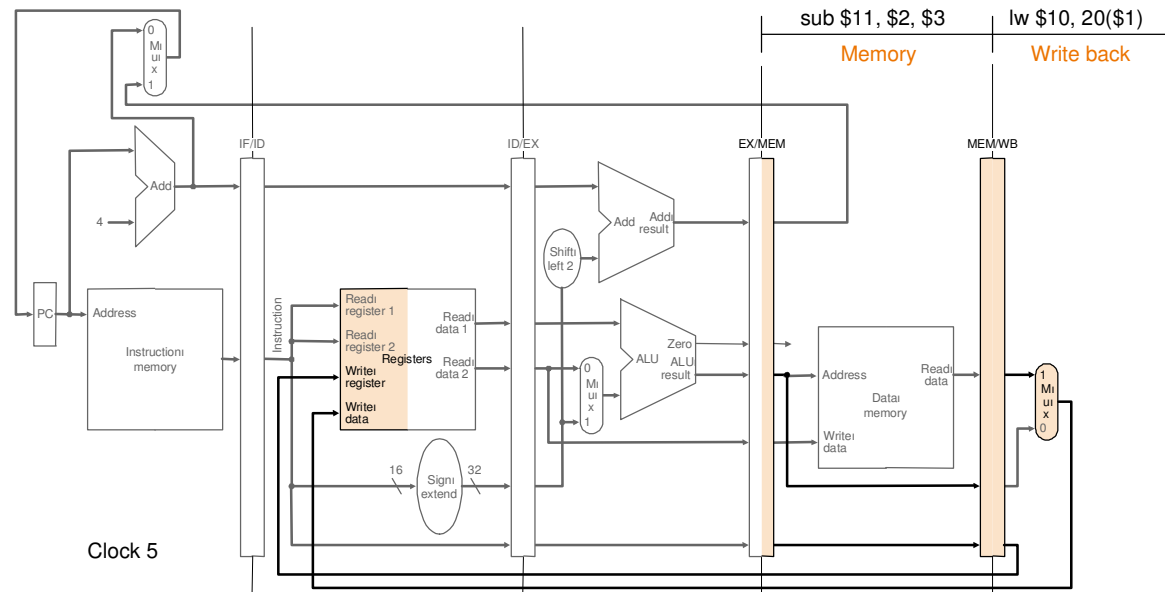
# Exemplo com sub e lw (1)



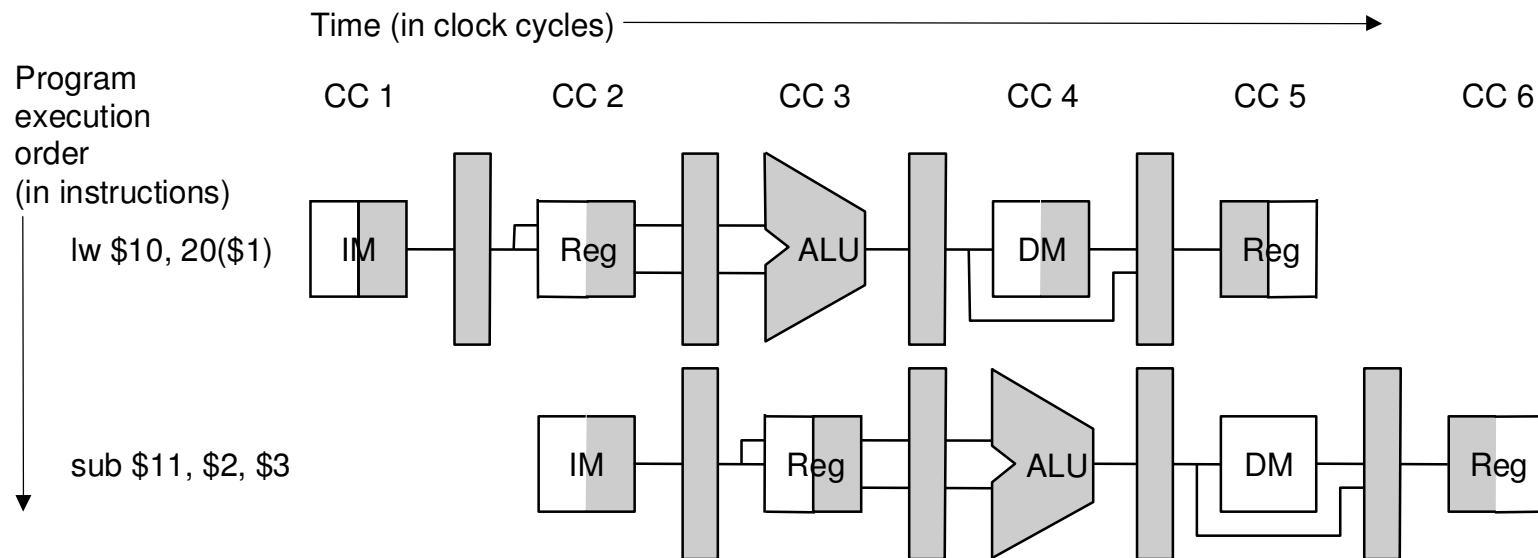
# Exemplo com sub e lw (2)



# Exemplo com sub e lw (3)



# Graphically Representing Pipelines



- **Can help with answering questions like:**
  - how many cycles does it take to execute this code?
  - what is the ALU doing during cycle 4?
  - use this representation to help understand datapaths