MC 602

IC/Unicamp

2011s2

Prof Mario Côrtes

VHDL

Latches e Flip-Flops

Tópicos

- Uso de processo e memória implícita
- Latches
- FFs
  - Reset síncronos e assíncronos

Descrições em VHDL

- Conceito importante: process

```
PROCESS ( A, B )
    BEGIN
            ……..   -- corpo do processo
    END PROCESS
```

- Trecho entre Begin e End é executado sequencialmente (a ordem importa)
- O processo é executado concorrentemente como as demais declarações
- O processo é invocado quando muda algum sinal/variável na lista de sensibilidade

Instanciação de FFD de um pacote

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
LIBRARY altera ;
USE altera.maxplus2.all ;

ENTITY flipflop IS
   PORT ( D, Clock  : IN      STD_LOGIC ;
       Resetn, Presetn : IN   STD_LOGIC ;
       Q         : OUT STD_LOGIC ) ;
END flipflop ;

ARCHITECTURE Structure OF flipflop IS
BEGIN
   dff_instance: dff PORT MAP
   ( D, Clock, Resetn, Presetn, Q ) ;
END Structure ;
```

Memória implícita

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY implied IS
   PORT (    A, B   : IN      STD_LOGIC ;
          AeqB   : OUT  STD_LOGIC ) ;
END implied ;

ARCHITECTURE Behavior OF implied IS
BEGIN
   PROCESS ( A, B )
   BEGIN
      IF A = B THEN
          AeqB <= '1' ;
      END IF ;
   END PROCESS ;
END Behavior ;
```

Latch tipo D chaveado

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY latch IS
   PORT (    D, Clk     : IN   STD_LOGIC ;
          Q   : OUT  STD_LOGIC) ;
END latch ;

ARCHITECTURE Behavior OF latch IS
BEGIN
   PROCESS ( D, Clk )
   BEGIN
       IF Clk = '1' THEN
          Q <= D ;
       END IF ;
   END PROCESS ;
END Behavior ;
```

Flip-Flop tipo D

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY flipflop IS
   PORT (    D, Clock   : IN   STD_LOGIC ;
          Q      : OUT  STD_LOGIC) ;
END flipflop ;

ARCHITECTURE Behavior OF flipflop IS
BEGIN
   PROCESS ( Clock )
   BEGIN
       IF Clock'EVENT AND Clock = '1' THEN
          Q <= D ;
       END IF ;
   END PROCESS ;
END Behavior ;
```

FFD com Wait Until

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY flipflop IS
    PORT (   D, Clock   : IN   STD_LOGIC ;
          Q   : OUT  STD_LOGIC ) ;
END flipflop ;

ARCHITECTURE Behavior OF flipflop IS
BEGIN
   PROCESS
   BEGIN
       WAIT UNTIL Clock'EVENT AND Clock = '1' ;
       Q <= D ;
   END PROCESS ;
END Behavior ;
```

FFD com Reset assíncrono

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY flipflop IS
   PORT (    D, Resetn, Clock     : IN  STD_LOGIC ;
          Q             : OUT  STD_LOGIC) ;
END flipflop ;

ARCHITECTURE Behavior OF flipflop IS
BEGIN
   PROCESS ( Resetn, Clock )
   BEGIN
      IF Resetn = '0' THEN
         Q <= '0' ;
      ELSIF Clock'EVENT AND Clock = '1' THEN
         Q <= D ;
      END IF ;
   END PROCESS ;
END Behavior ;
```

FFD com Reset síncrono

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY flipflop IS
   PORT (    D, Resetn, Clock     : IN   STD_LOGIC ;
          Q             : OUT  STD_LOGIC) ;
END flipflop ;

ARCHITECTURE Behavior OF flipflop IS
BEGIN
   PROCESS
   BEGIN
       WAIT UNTIL Clock'EVENT AND Clock = '1' ;
       IF Resetn = '0' THEN
          Q <= '0' ;
       ELSE
          Q <= D ;
       END IF ;
   END PROCESS ;
END Behavior ;
```