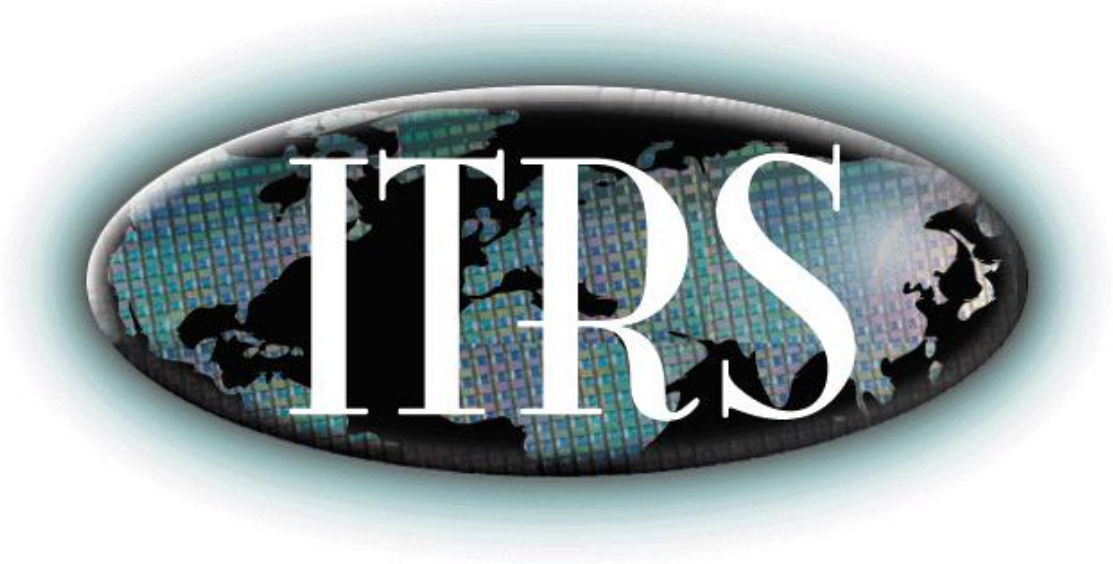

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

EXECUTIVE SUMMARY

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INTRODUCTION

OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A *Improvement Trends for ICs Enabled by Feature Scaling*

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 30 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005) [which now includes Analog technology emphasis and enhancements], Emerging Research Materials, to better reflect this evolution of the semiconductor industry (2007), and new in 2011, a Microelectromechanical Systems (MEMS) chapter [also aligned with the international Electronics Manufacturing Initiative (iNEMI) Roadmap] . The ITRS 2010 Update also began to address the subject of Energy, which also includes additional emphasis in the 2011 ITRS Factory Integration chapter

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

In order to properly represent the continuously evolving facets of the semiconductor industry as it morphs into new and more functional devices in response to the broadening requirements of new customers, the 2007 ITRS has addressed the

concept of Functional Diversification ("More than Moore"). This new definition (MtM) addresses an emerging category of devices that incorporate functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP), chip-level (SoC) Stacked Chip SoC (SCS) solution. The new Microelectromechanical Systems (MEMS) chapter also supports the ITRS MtM analysis with guidance for sensor and actuator technologies.

It is forecasted that by the end of this next decade (2019) it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensure that the 2011 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete ITRS 2011 Renewal and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site http://www.itrs.net.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.). The principal IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS Workshops
- Editing the ITRS

The International Technology Working Groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2011 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging
- Microelectromechanical Systems (MEMS) – new for the 2011 ITRS

Crosscut ITWGs are the following:

- Emerging Research Materials

- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

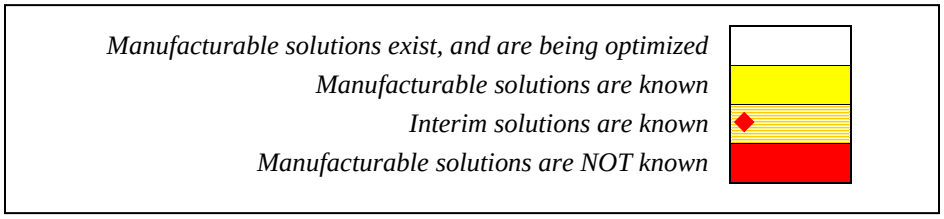
For the 2011 edition, three ITRS meetings were held worldwide as follows: Potsdam, Germany, (sponsored by the ESIA and hosted by Infineon); San Francisco, U.S.A., sponsored by the SIA, organized by SEMATECH and co-hosted with SEMI/North America; and Incheon, Korea (sponsored and co-hosted by KSIA and Samsung). These meetings provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the different ITWGs. In addition, the ITRS teams hold public ITRS conferences bi-annually to present the latest Roadmap information and to solicit feedback from the semiconductor industry at-large.

The ITRS is released annually, with updates and corrections to data tables each even-numbered year (such as 2000, 2002, 2004, 2006, 2008, 2010) while complete editions are released each odd-numbered year (2001, 2003, 2005, 2007, 2009, 2011). This ITRS process thus ensures continual assessment of the semiconductor industry's near and long-term needs. It also allows the teams to correlate in a timely fashion the ITRS projections to most recent research and development breakthroughs that may provide solutions to those needs.

ROADMAP CONTENT

The ITRS assesses the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity and confidence levels, represented by colors in the tables, for these targets:



The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

As indicated in the overview, the Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge" spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS road-mapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

TECHNOLOGY CHARACTERISTICS

As mentioned above, a central part of the IRC guidance and coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics tables. Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the 2007 ITRS, the ORTC and technology requirements tables are fully annualized and in both the "Near-term Years" (2011, 2012… through 2018) and "Long-term Years" (2019, 2020 … through 2026) This format is illustrated in Table B, which contains a few key rows from lithography-and-process-related Table ORTC1, including the Flash product uncontacted polysilicon half-pitch technology trend line item as the most aggressive technology target. In the previous 2005 Roadmap editions, the DRAM stagger-contacted M1 half pitch line item was used as a standard header for all the ITRS ITWG tables; however, beginning with the 2007 edition, the IRC has requested that only the year of first production be required as a standard header. At the discretion of the ITWGs, other product technology trend driver line items may be selected from Table ORTC1 for use in their ITWG tables as overall headers indicating key drivers for their tables.

Table B ITRS Table Structure—Key Lithography-related Characteristics by Product

Near-term Years

Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14.2	13.0	11.9
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18.9	16.9	15.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19.8	17.7	15.7
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15.3	14.0	12.8
ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	41	35	31	25	22	19.8	17.7	15.7
ASIC/Low Operating Power Physical Gate Length (nm)[1]	26	24	21	19.4	17.6	16.0	14.5	13.1
ASIC/Low Standby Power Physical Gate Length (nm)[1]	30	27	24	22	20	17.5	15.7	14.1
MPU High-Performance Etch Ratio GLpr/GLph [1]	1.4589	1.4239	1.3898	1.3564	1.3239	1.2921	1.2611	1.2309
MPU Low Operating Power Etch Ratio GLpr/GLph [1]	1.5599	1.4972	1.4706	1.2869	1.2640	1.2416	1.2196	1.1979

Long-term Years

Year of Production	2019	2020	2021	2022	2023	2024	2025	2026
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	10.9	10.0	8.9	8.0	8.0	8.0	8.0	8.0
DRAM ½ Pitch (nm) (contacted)[1,2]	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	13.4	11.9	10.6	9.5	8.4	7.5	6.7	6.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	14.0	12.5	11.1	9.9	8.8	7.9	6.79	5.87
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	11.7	10.6	9.7	8.9	8.1	7.4	6.6	5.9
ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	14.0	12.5	11.1	9.9	8.8	7.9	6.8	5.8
ASIC/Low Operating Power Physical Gate Length (nm)[1]	11.9	10.8	9.8	8.9	8.1	7.3	6.5	5.8
ASIC/Low Standby Power Physical Gate Length (nm)[1]	12.7	11.4	10.2	9.2	8.2	7.4	6.6	5.9
MPU High-Performance Etch Ratio GLpr/GLph [1]	1.2013	1.1725	1.1444	1.1169	1.0901	1.0640	1.0315	1.0000
MPU Low Operating Power Etch Ratio GLpr/GLph [1]	1.1766	1.1558	1.1352	1.1151	1.0953	1.0759	1.0372	1.0000

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Please refer to the Glossary for detailed definitions for Year of Introduction and Year of Production.

TECHNOLOGY PACING

In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes. However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver, including DRAM

For example, along with half-pitch advancements, design factors have also rapidly advanced in Flash memory cell design, enabling additional acceleration of functional density. Flash technology has also advanced the application of electrical doubling of density of bits, enabling increased functional density independent of lithography half-pitch drivers. A second example is given by the MPU/ASIC products, for which the speed performance driver continues to be the gate-length isolated feature size, which requires the use of leading-edge lithography and also additional etch technology to create the final physical dimension.

Significant confusion relative to the historical ITRS node definition continues to be an issue in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria. Of course, we now expect different IC parameters to scale at different rates, and it is certainly legitimate to recognize that many of these have product-specific implications. In the 2011 ITRS, we will continue the practice of eliminating references to the term "technology node." As mentioned above, the IRC has recommended that the only standard header will be year of first production, and DRAM M1 half-pitch is just one among several historical indicators of IC scaling. With this latest change to standard ITRS table format policy, it is hoped that the ITRS will not contribute to industry confusion related to the

concept of "technology node." Of course, "node" terminology will continue to be used by others. Hopefully, they will define their usage within the context of the application to the technology of a specific product.

For reference on the 2011 ITRS common definition of M1 half-pitch for all products, as well as the definition of polysilicon half-pitch for FLASH memory, see Figure 1.

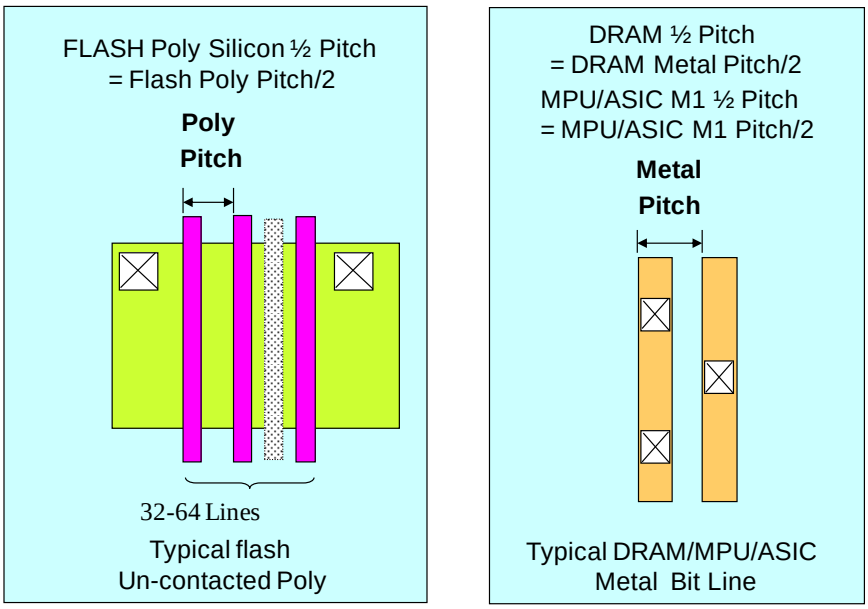


Figure 1 2011 Definition of Pitches

MEANING OF ITRS TIME OF INTRODUCTION

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production," which is defined in Figure 2.

Figure 2 was revised in the 2009 ITRS to no longer include reference to volume parts per month, due to the variability of different product die sizes for first production targets. Therefore, only the typical industry high volume ramp scale is retained in the 2011 roadmap.

A graphical note is included, at the request of the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) TWGs. . The note is a reminder of the very-wide-time-range required to capture early research activities that may result in Potential Solutions items for the ITWG Grand Challenges. It has become increasingly important to communicate a broad horizon encompassing both the period preceding the first manufacturing alpha tools and materials and also the period that extends to the classic ITRS 15-year horizon and even beyond.

The preceding horizon is required to capture the period of the very first technical conference paper proposals until the start of development activities; at which point typically a transfer from ERD/ERM to PIDS/FEP ITWGs occurs. The early research horizon also reminds the readers and the ITRS participants of the influence of the National Technology Roadmap for Semiconductors (NTRS: 1991-1998) and the International Technology Roadmap for Semiconductors (ITRS: 1998 to present), as the work of the roadmaps tracked and influenced the manufacturing technology needs and priorities of industry R&D long before they turn into production. Many academic and industry studies have examined and commented on the uniqueness and the impact of pre-competitive cooperation provided by the International Technology Roadmap for Semiconductors.

For more explicit clarification of the ERD/ERM long-range timing s-curve, see Figure 3, in which an example is shown for a new gate structure potential solution targeted for 2019 production. In this example, the first research papers appeared

in 2007, and the Potential Solution technology was transferred to PIDS during the 2011 ITRS roadmap work, when more detailed line item characteristics were defined by the PIDS TWG in their 2011 chapter

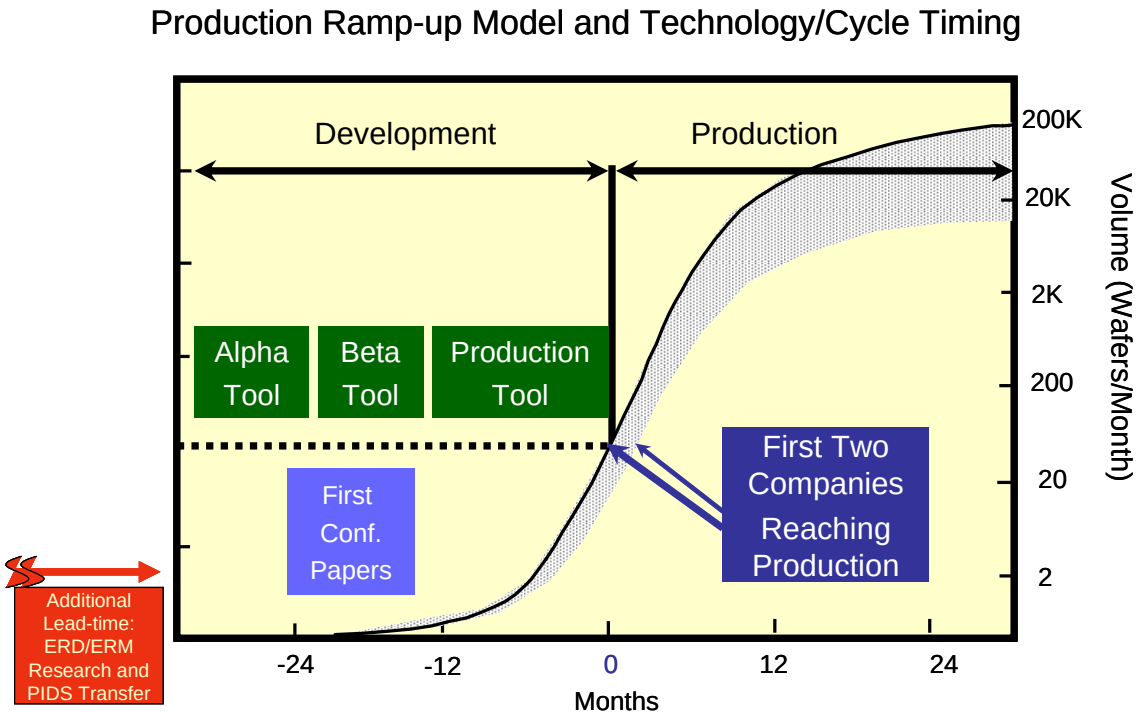


Figure 2 *A Typical Technology Production "Ramp" Curve (within an established wafer generation)**

**see Figure 3 below for ERD/ERM Research and PIDS Transfer timing; and also Figure tbd-4 (in 450 mm topic) for Typical Wafer Generation Pilot and Production "Ramp Curves"*

The "Production" time in the ITRS refers to the time when the first leading company brings a technology to production. Typically, a second company follows within a short period of time, and ideally as soon as three months; however sometimes there is a longer time for the second company to get into production, especially when considering alternative "equivalent scaling" technology pathway options (see Equivalent Scaling topic). Additional complexity of timing occurs when rapid accelerations occur, and a leading company will go into production ahead of the ITRS Roadmap timing targets. This happened in the case of MugFET production announcements in 2011 (from 2015), and there is the possibility of III/V Ge technology acceleration to 2015 (from 2019), which must be included in the 2012 ITRS Update work (also see Equivalent Scaling topic). It remains to be seen how rapidly "fast following" companies provide their own announcements in response to production accelerations, and updates on this topic will be discussed by the IRC and included in the 2012 Update work.

For further clarification,"production" means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figures 2 and 3 can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM to full capacity can take nine to twelve months. As an example, this time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month [for the example of a chip size at 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month)].

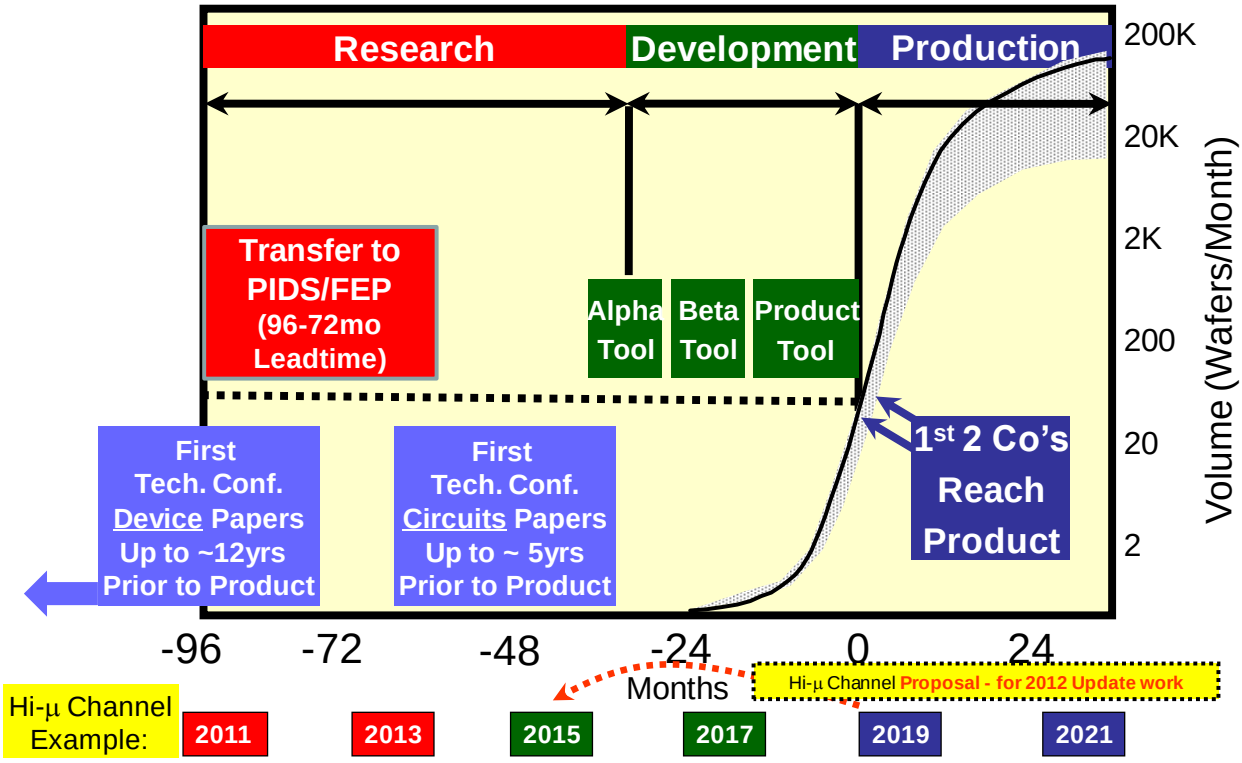


Figure 3 A Typical Technology Production "Ramp" Curve for ERD/ERM Research and PIDS Transfer timing (including an example for III/V Hi-Mobility Channel Technology Timing Scenario – also see the Equivalent Scaling topic)

2011 SICAS INDUSTRY MANUFACTURING TECHNOLOGY CAPACITY UPDATE

It is noted that the ITRS, by its definition, focuses on forecasting the earliest introduction of the leading-edge semiconductor manufacturing technologies, which support the production of selective leading-edge driver product markets, such as DRAM, Flash, MPU, and high-performance ASICs. It is, however, true that many companies, for a variety of reasons, may choose to introduce a leading-edge technology later than the earliest introduction of the leading-edge technology; hence, there is a wide variation of the technologies in actual production status from leading edge to trailing edge.

Furthermore, it has been observed that some companies consciously choose to utilize aggressively leading-edge technologies only for a subset of their product portfolio; because it is not economically attractive to do so for all products. Individual Companies decide to go slower or even stick to trailing technologies with specific products because further shrinking might not even make sense anymore. Therefore there appears to be a broader split of technologies in use which is becoming even broader.

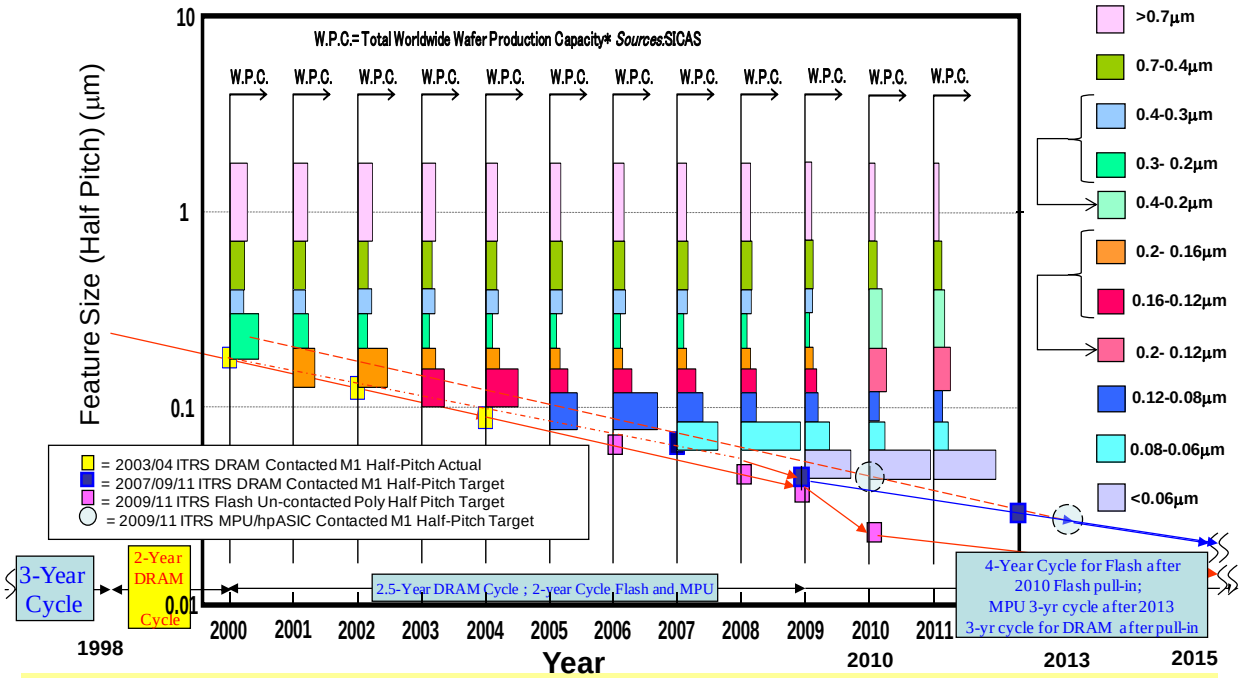
Figure 4 [updated with 4Q11 SICAS data] shows, in horizontal bar graph format (each bar width is proportional to silicon processing capacity), the actual, annual worldwide wafer production technology capacity distributions over different process feature sizes. The distributions of the overall industry technology capacity segments are tracked by feature-size splits..

Note that the first production of the leading-edge feature size has historically ramped into a 20–30% industry capacity share within one year, and the timing of that 20–30% capacity share has been on the same cycle as the same historical two-year-pace timing for first production. However, the latest SIA WSTS statistics for the "<0.06μm" technology demand split [added to the worldwide semiconductor trade statistics (WSTS) survey in 2009] indicate that the average industry demand pace continues at the most-leading-edge capacity on the two-year demand pace.

Furthermore, the relative percentage of the most leading-edge technology capacity has been rapidly growing. The combined capacity of the most recent two technology generations has typically grown to nearly half the capacity of the industry within two to three years after their introduction. It can be observed in Figure 4 that the capacity for the most leading edge technology (32 nm) is presently only available within the SICAS "<0.06µm" capacity split. The availability of the "<0.04 µm" split survey data, which would include the rapidly ramping 32 nm Flash and MPU/ASIC technology cycle capacity, is not expected from SICAS surveyors and their participants until late in 2011. Therefore, the actual analysis of the 1.5-year to three-year technology demand cycles (to the 20–30% of total MOS capacity ramp point) will not be available until possibly the 2012 Update of the ITRS.

It is notable that relative share of trailing edge capacity does not decline as rapidly as might be expected (migrate upward to leading-edge); and the leading-edge capacity split shares should be expected to continue to compete with one another as products migrate to the most leading-edge capacity ("<0.06 µm" capacity data). This phenomenon continues to hold significant implication for the markets and business models of the materials and equipment suppliers that ultimately develop and deliver the required solutions to the ITRS technology Grand Challenges.

Suppliers must provide support for not only the longer-lasting trailing edge factories, but also the many diverse product and technology factories at the leading edge. In addition, suppliers must deliver alpha and beta tools and materials two to three years ahead of the first production requirement, and then they must be prepared to ramp into production with overlapping technology demand capacities. These scenarios present both a market opportunity and also an R&D and support resource challenge to both suppliers and manufacturers, especially with the preparation for 450 mm wafer generation investments.



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 1Q data for 2011. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

Figure 4 *Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution*[1]

[1] *The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of 1Q11. The detailed data are available to the public online at the SIA website, www.sia-online.org, and data is located at http://www.sia-online.org/industry-statistics/semiconductor-capacity-utilization-sicas-reports/*

ROADMAP SCOPE

Traditionally, the ITRS has focused on the continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, since 2001, we have reached the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 6 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the ITRS must address post-CMOS devices. The Roadmap is necessarily more diverse for these devices, ranging from more familiar non-planar CMOS devices to exotic new devices such as spintronics. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. In addition, product performance increasingly does not scale only with the number of devices, but also with a complex set of parameters given by design choices and technology. Thus new technologies may involve not only new devices, but also new manufacturing and design paradigms.

Microprocessors, memories, and logic devices require silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many quantitative requirements, such as power consumption and communications bandwidth (e.g., RF), and many functional requirements, such as the functions performed by passive component, sensors and actuators, biological functions, and even embedded software functions, do not scale with Moore's Law. In many of these cases, non-CMOS solutions are employed. In the future, the integration of CMOS- and non-CMOS based technologies within a single package (or system-in-package, (SiP)) will become increasingly important. In terms of functionality, SoC and SiP can be complementary, and hence are not necessarily competing with each other. Functions initially fulfilled by non-CMOS dedicated technologies may eventually be integrated onto a CMOS SoC, using mixed technologies derived from core CMOS. Consequently, the partitioning of system-level functions between *and within* SoC and SiP is likely to be dynamic over time. This will require innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, extremely parallel software, etc. For SiP applications, packaging will be a functional element and a key differentiator. This trend is represented graphically in the 2009 ITRS Figure 5.

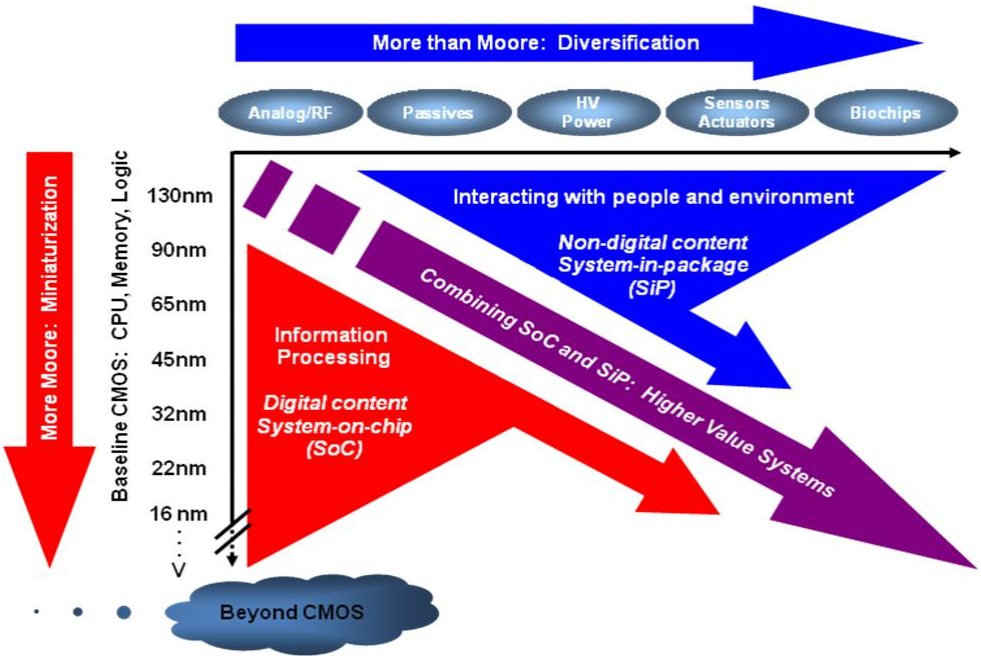


Figure 5 Moore's Law and More

These concepts," introduced in the 2005 roadmap, have been further discussed and refined since. In particular, consensus was reached on the following definitions. (Refer to Figure 5 and the Glossary):

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling*—refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)*—refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)*—refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: design-for-variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multi-core SOC architectures."
    - Addresses the need for quantifiable, specific design technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs; and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution. In addition to technology developments, this trend requires the development of many enabling techniques such as (not exhaustive) heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology.

Beyond CMOS—emerging research devices (ERD) and Materials (ERM), focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switches, and nano-electro-mechanical-system (NEMS) switches.

It is expected that the relative weight of the "More than Moore" component of the industry evolution will increase over time. This increase leads to a growing diversity of the scientific fields that the research must cover in order to sustain the pace of innovation, while the financial constraints are becoming tighter. The question of the guidance of the research efforts, in which the ITRS is playing a pivotal role, is therefore crucial. Given the benefits that roadmapping has brought to the semiconductor industry so far, the International Roadmap Committee clearly wants to include more significant parts of the "More-than-Moore" domain in the work of the ITRS community. In particular, it has tackled the difficult question of how to build a roadmap (or several roadmaps) for the various "More than Moore" technologies. Indeed, in the absence of a single law of expected progress such as Moore's law for the many devices and technologies that enable the "More than Moore" trends, a different methodology is needed to identify and guide roadmap efforts in the MtM domain.

The ITRS has therefore elaborated a white paper, *available at this link on the ITRS website (http://www.itrs.net/papers.html)*, to propose a methodology that helps the ITRS community to identify those MtM technologies for which a roadmapping effort is feasible and desirable. It departs from the traditional "technology push" approach that the ITRS has followed for roadmapping the continuation of Moore's law (i.e., linear scaling), and requires to collect both technical and market data, thus implying the involvement of many actors beyond the ITRS historical membership, and representing the application domains.

It should be stressed here that the white paper is not intended to be the "final words" on MtM roadmapping methodology, but rather a way to collect more inputs and advices on what promises to be a very challenging task. Illustrating this point was the first More than Moore workshop held after the 2011 April ITRS meetings in Potsdam, Germany.

Without even waiting for the outcome of that work, various working groups of the ITRS have been investigating the consequences of the "More than Moore" trend in their field of expertise. The results of that work, which will further gain momentum in the coming years, can be found in their respective chapters, We can also recall here the white paper which was developed by the Assembly and Packaging TWG, and placed on the public website to provide more details on the system-on-chip (SOC) and system in package (SIP) concepts.

Finally, to increase the emphasis and connection to industry "complete solutions," and the technology and manufacturing solutions required by future applications, the 2011 ITRS has added a MEMS chapter to the roadmap, and also aligned it with previous work included in the 2011 international Electronics Manufacturing Initiative (iNEMI) roadmap.

In parallel, the "Beyond CMOS" concept has been given more discussion and detail in the ERD and ERM chapters.

To summarize, the scope of the 2011 ITRS specifically includes detailed technology requirements for all CMOS integrated circuits, including wireless communication and computing products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies, even though that is not the explicit purpose of the Roadmap.

2011 ITRS SPECIAL TOPICS

TRANSITION TO 450 MM –A STATUS UPDATE FOR THE 2011 ITRS

The rationale for a transition to 450 mm diameter wafer is productivity, one of the enablers of Moore's law. This is the ability—everything else staying the same—to decrease the manufacturing cost of each mm^2 of IC by the use of larger diameter wafers. Based on economic considerations, during the 2007 ITRS roadmap development, the International SEMATECH Manufacturing Initiative (ISMI) had determined that to stay on this productivity curve, the industry needed to achieve 30% cost reduction and 50% cycle time improvement in manufacturing, which in their opinion would be achievable only via a transition to 450 mm (while the cost reduction goal has been achieved through previous wafer generation changes, the cycle time goal is new). The need for 450 mm wafer generation transition productivity was reinforced in 2007 by the conclusions of an analysis of potential 300 mm improvements, which showed that the so-called "300 mm Prime" program had cycle time opportunity but fell short of the traditional cost reduction required to stay on Moore's Law. This realization prompted ISMI to kick-off the 450 mm initiative in July 2007.

Subsequently, Intel, Samsung, and TSMC (IST) announced in May 2008 that they would work together with suppliers, other semiconductor players, and ISMI to develop 450 mm with the original goal set in 2008 for a consortium pilot line in 2012, which would support Integrated Device Manufacturers (IDM) and foundry pilot line development in the 2013-14 timeframe, followed by first production ramps in the 2015-16 timeframe.[2]. The 2008 public announcement and assessment was the statement of record by these three companies and ISMI and used in the writing of the ITRS 2009 and 2010 editions. Additionally, it was subject to revision based on future statements and required updating to the latest status and approach of the consortium.

Taking lessons from the past, it can be observed that each wafer size transition has been different from any of the previous ones. The conversion to 300 mm wafer can be characterized by fact that for the first time the consortia (I300I and Selete) led the whole industry effort. The well-tested consortium effort is now also the chosen approach for enabling the 450 mm wafer size conversion. SEMI participation was also essential in the 300 mm wafer size conversion since for the first time "provisional standards" were agreed upon by the whole industry before the final manufacturing equipment was fully developed. In particular, the industry solved a fundamental problem by agreeing on adopting full wafer transport automation. All the suppliers abandoned their proprietary solutions to wafer transport, port design, and load size in favor of the agreed FOUP/ overhead solution. This effort took many years of discussion before the final solution was finally agreed by all parties.

In this respect, the 450 mm wafer size transition is taking full advantage of the work previously done to standardize the 300 mm wafer transport by having already adopted the same whole automation scheme with only minor upgrades - thus placing the 450 mm silicon standards and automation schedule ahead of the corresponding 300 mm wafer size conversion schedule with respect both to automation and also to silicon material standards. During the interim consortium work since the 2009 ITRS publication, consortium progress has resulted in the completion of international standards for 450 mm

[2] *Source: "May 2008"/ "Oct 2008 ISMI symposium"/Dec'08 ISMI 450 mm Transition Program Status Update for ITRS IRC,Seoul,Korea*

carriers, loadports, and developmental test wafers. These advances were enabled by extensive prototyping and interoperability / cycle testing in cooperative development between component Suppliers, SEMI and ISMI.

During 2011, significant development progress was achieved by consortia and is ongoing, as is dialogue between semiconductor manufacturers and suppliers to assess standards and productivity improvement options on 300 mm and 450 mm generations. Economic analysis of option scenarios was also advanced in order to examine the required R&D cost, benefits, and return-on-investment, along with funding mechanism analysis and proposals from companies, and different regional consortia and governments.

2011 witnessed the move of the SEMATECH 450 mm program from Austin, Texas, to Albany, New York, where a new consortium clean room is under construction for continued alpha and beta tool development and preparation for IDM and foundry pilot line demonstrations. In addition, the European EEMI 450 mm consortium initiative was announced, with targets for 450 mm development in new facilities in IMEC in Belgium. Most recently a private consortium initiative was announced, identified as the Global 450 mm Consortium (G450C), by five major industry players—Intel, Samsung, TSMC, GLOBALFOUNDRIES, and IBM to invest $4.4B to advance 450 mm manufacturing and technology development. Although much work remains over the next several years, these announced large investment commitments, and with potentially more coming from the EEMI 450 mm consortium, will go far to support the globally-coordinated effort needed to ensure a cost-effective and timely transition to the next wafer size.

Given all of the above, [and with possible advancements based on the work of Next Generation Factory (NGF) programs at SEMATECH/ISMI that may create opportunities for improvement of 300 mm equipment which might eventually also be applicable to 450 mm processing], the ITRS IRC now expects that consortium development and demonstration work will continue, supporting the development of material and manufacturing tools to be available between 2013 to 2014 for IDM and Foundry pilot lines...If the announced targets by IDM and Foundry pilot lines remain on track for 2013-14, then the ITRS target for 450 mm production manufacturing ramp from 2015–2016 should also be possible, subject to 450 mm wafer high volume availability. The ITRS/IRC continues to recommend that wafer diameter should not be tied to technology generations—leading edge technologies will for a limited period be running both in 300 and 450 mm technologies, as happened with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm-130 nm M1 half-pitch) timeframe.

To support the latest industry status, in the 2011 ITRS an updated version of the 450 mm Production Ramp-up Model Graphic has been provided (Figure 6) to clarify the special dual "S-curve" timing required when a new wafer generation is being introduced [modeled after the experience with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm-130 nm M1 half-pitch) timeframe].

Note that the 2011 ITRS revision wafer generation timing targets for the 450 mm generation remain fundamentally unchanged from the 2009 and 2010 ITRS. The International Roadmap Committee (IRC) had originally indicated, in the 2009 ITRS, a 450 mm volume production ramp in the 2014–2016 time frame, and that range is narrowed to 2015–16 in this 2011 ITRS edition and shown in the timing graphic.

Although the timing targets for 450 mm, IDM and Foundry pilot line and production ramp timing remain fundamentally unchanged, please note the clarifications added to the consortium work timing, which now includes 450 mm equipment development and demonstration, but does not include a full-flow consortium pilot line. It is now believed by the consortium IDM and Foundry members that only demonstration support is required from the consortium; and that final full-flow beta and production development should occur in IDM and Foundry company pilot lines in the 2013-14 timeframe. Announced plans continue to support the original targets for 450 mm production ramp in the 2015-16 timeframe for 1× node technology manufacturing (15-16 nm Flash Poly half-pitch, 20-22 nm M1 half-pitch DRAM and MPU/ASIC 2011 ITRS technology targets).

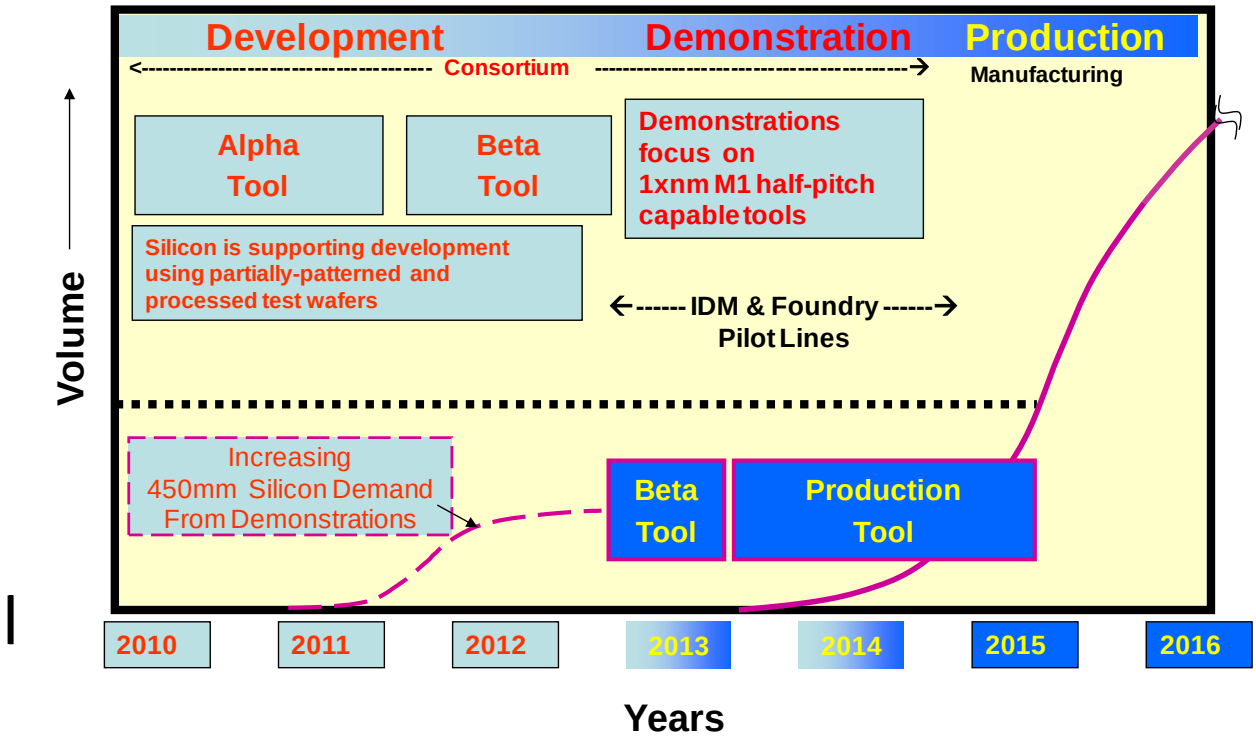


Figure 6 *A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation*

For completeness of the 2011 ITRS 450 mm status, and as a service to the readers, it should also be noted that significant progress on economic modeling scenarios was also achieved by SEMATECH/ISMI, including updating and enhancing the ISMI Industry Economic Model (IEM); and also including contracting with a well-known industry consultant, IC Knowledge (ICK)[3] to develop a strategic-range model of equipment demand. That ISMI and ICK model work was based on the ITRS 2009 ITRS and 2010 Update.

LITHOGRAPHY MASKS COUNT – A STATUS UPDATE FOR THE 2011 ITRS

A need was identified during the 2009 ITRS work to update the Lithography Masks Count driver in the Overall Roadmap Technology Characteristics (ORTC) Table 5. With the rapid emergence of multiple-patterning exposure in the leading-edge technology product manufacturing processes, it was decided by the Lithography ITWG to do a survey of its ITWG participants and SEMATECH consortium members in order to refresh the estimates of trends for masks count in the various product categories.

Consequently, during the year 2010, a survey was completed that would enable a revision. The data from that work can be viewed in the *2011 Table ORTC-5: Electrical Defects and Lithography Mask Levels.* Due to limited participation by DRAM companies in this survey, the Lithography TWG used the MPU data to estimate the DRAM masks count. The data for all product categories is plotted in a graph below, Figure 7.

The trends for all products are increasing dramatically due to increasing process technology complexity and the application of multi-patterning lithography. The respondents to the survey also indicate an equally dramatic effect with the assumption of using Extreme Ultra-Violet (EUV) technology in production. [2011 ITRS Litho TWG consensus for EUV timing: DRAM/2013; Flash/2013; MPU: 2015].

Note that due to the visibility limit of Flash product survey respondent to 2014, they did not provide data on the impact of future Flash 3D cell layer technology (ITRS production timing 2016 and beyond). However, see additional comments below on modeled visibility of 3D Flash.

[3] *Special acknowledgment to Scott Jones with IC Knowledge for his contributions towards the 2011 ITRS effort.*

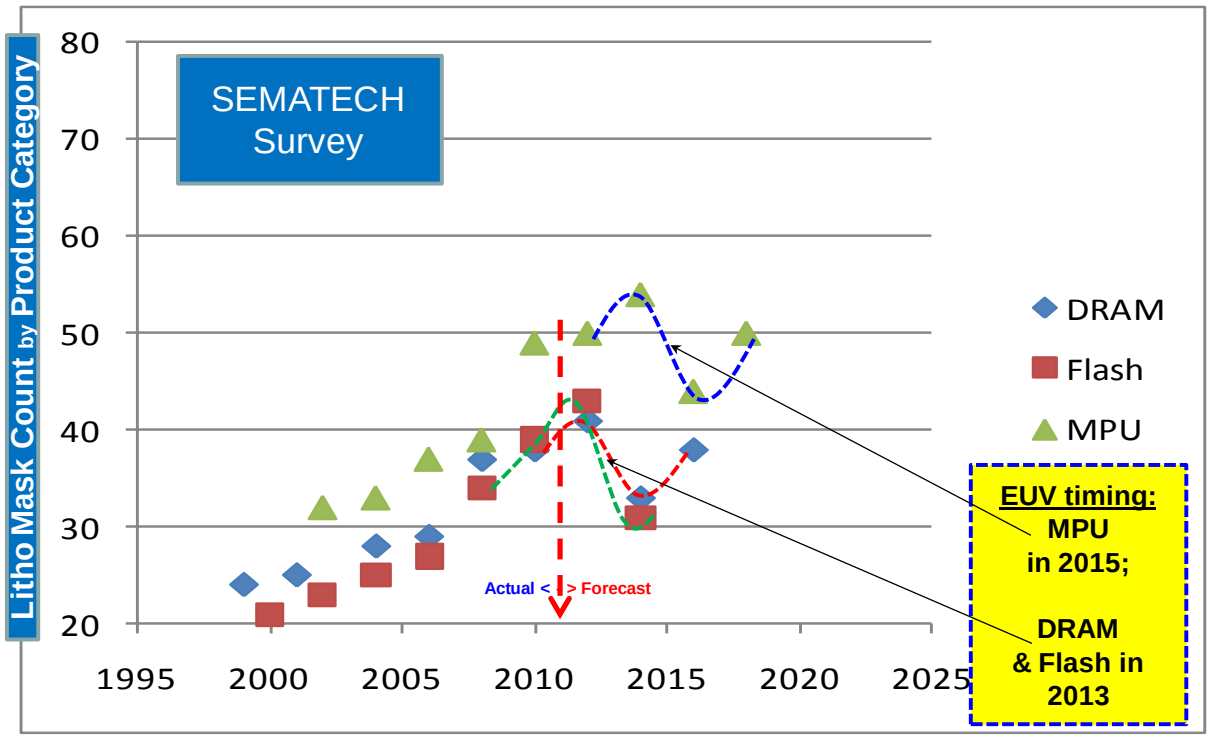


Figure 7 *Lithography Masks Count by Product Category – Litho TWG & SEMATECH Survey*

Also available to the Lithography TWG in their 2011 ITRS work, and now to ITRS readers, was analysis provided by IC Knowledge (ICK), which was based on the ICK commercial Strategic Model. The ICK Strategic Model was developed in cooperation with SEMATECH and the ITRS TWGs, and is based upon the 2009 and 2010 ITRS editions. The ICK model builds product-based (ITRS MPU, DRAM, NAND Flash) process flow scenarios from the ITRS near and long-term technology timing (see Figure 8).

From the masking levels in the scenario process steps/levels, and using the latest 2011 ITRS edition Lithography TWG timing for exposure technologies [multiple-masking, Extreme Ultra-Violet (EUV)], the ICK model can generate estimates of the mask counts and demonstrate the impact of new technology insertion. Unlike the limited timing of the survey responses, this additional ICK-modeled scenario visibility is able to be applied across the full range of 2011-2026. Since the ICK model is based on scenario process flows, rather than survey-response data, the results vary from the Lithography TWG survey results. However the model results are similar and consistent with the survey results, enabling validation as well as timing extension for comparison.

Also the ICK model scenario assumptions can be varied, to examine the impact of a delay of technology insertion. For example, if EUV were delayed two years from 2015 to 2017, the number of masks count peak in 2015 (65 masks count) increases to nearly 80 masks count peak in 2017.

Furthermore, the model analysis has been provided by ICK to enable readers of the ITRS to evaluate the cost impact of masks count increases, such as the delay of EUV. Other impact on Flash technology has also been provided, such as the possible savings of masks count by the use of charge trap technology in 2012; or the dramatic increases anticipated by the use of Flash 3D cell layer technology in 2016, possibly growing from 8 layers to 128 layers by the end of the roadmap range (raising masks count from a low of 30 in 2014 to 50 in 2024).

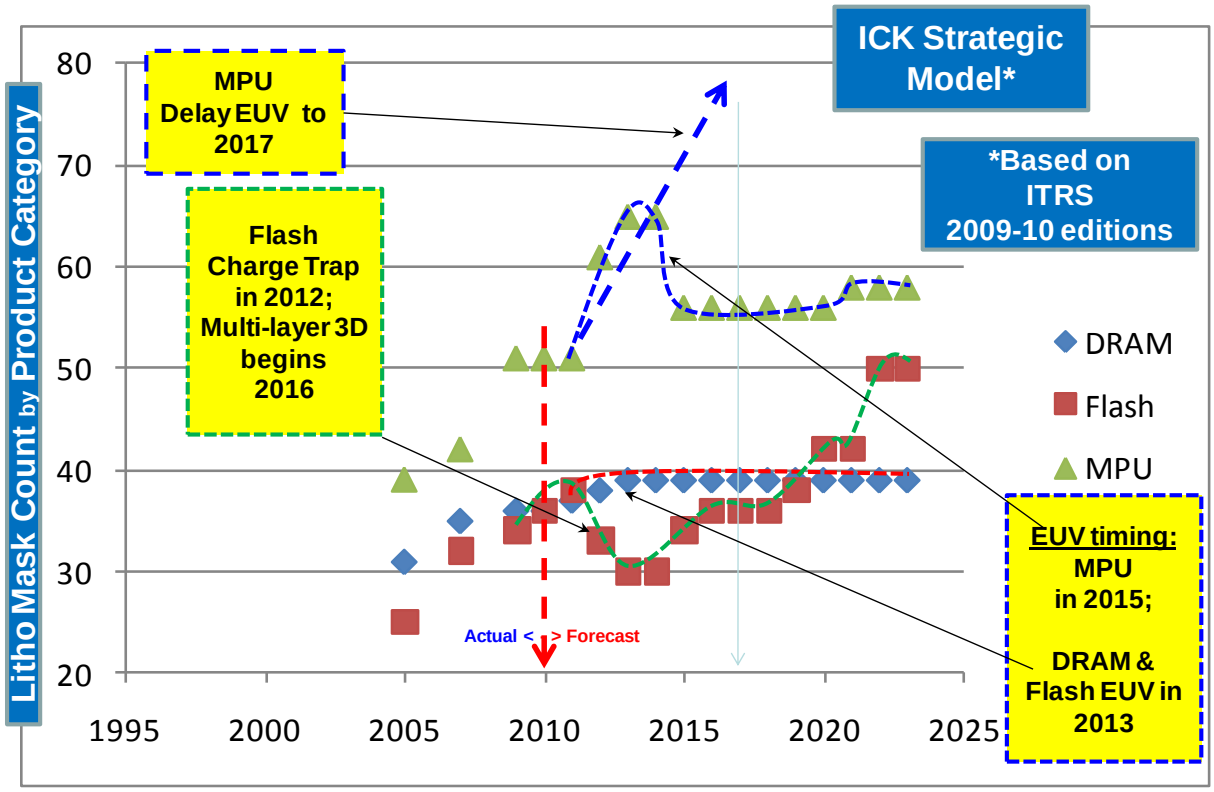


Figure 8 *Lithography Masks Count by Product Category – ICK ITRS Process Model-based Scenarios*

Clearly the availability of the new lithography masks count data, from both the survey and model work, adds significant visibility and utility to the ITRS, and enables the assessment by all TWGs on the impact of the ITRS timing of the industry grand challenges and potential technology solutions. The Yield Enhanement (YE) ITWG, in particular, is undertaking work on the 2012 ITRS Update to model the impact of the new masks count data upon the defect density (D_0) targets. The YE D_0 targets in the ORTC Table 5 were not adjusted to take into account the latest masks count data from Lithography work and is not indicated in this table; however, additional YE D_0 modeling is planned for update in 2012.

POWER AND ON-CHIP FREQUENCY PLANS

FREQUENCY AND POWER PIDS AND DESIGN CROSS-TWG WORK

Cross-TWG work between PIDS and Design is a part of every new ITRS edition, and the 2011 ITRS is no exception. This year's cross-TWG work has included an update of the Design TWG driver for on-chip maximum frequency, and also an update to the PIDS Vdd, and High Performance, and Low Operating and Standby Power targets. PIDS table updates also includes alternative process "equivalent scaling" pathway line items as tradeoffs with the historical dimensional solutions provided by shorter dimensional physical gate lengths (GLph) and equivalent oxide thickness (EOT).

The Design TWG need-driver trend for on-chip frequency was last updated during the 2008 ITRS, when survey work and analysis of the industry status was completed.

In 2011, a new Design TWG proposal was accepted to begin the driver basis at 3.6 Ghz, and grow the frequency throughout the roadmap range at a compound annual growth rate (CAGR) rate of 4%. This new trend was a significant reduction from the original 2008 ITRS trend (starting level of 4.70Ghz/2007 and growth rate of 8% (model 7.72% CAGR). The comparison of the 2009/10 ITRS Design Max Frequency targets versus the latest targets in the ORTC Table 4 can be seen below in the Table C.

Table C 2011 Chip Frequency Model Trend vs.2009/2010 ITRS Frequency

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
Chip Frequency (MHz) On-chip local clock -- WAS	5.454	5.875	6.329	6.817	7.344	7.911	8.522	9.180	9.889	10.652
Chip Frequency (MHz) On-chip local clock – 2011 IS*	*3.462*	*3.600*	*3.744*	*3.894*	*4.050*	*4.211*	*4.380*	*4.555*	*4.737*	*4.927*

Year of Production	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	2025	2026
Chip Frequency (MHz) On-chip local clock -- WAS	11.475	12.361	13.315	14.343	15.451	16.640	-	-
Chip Frequency (MHz) On-chip local clock – 2011 IS*	*5.124*	*5.329*	*5.542*	*5.764*	*5.994*	*6.234*	*6.483*	*6.743*

** Design ITWG*

The new 2011 ITRS On-chip Frequency trend provides a large "headroom" for designers and the original 2008 ITRS PIDS modeled intrinsic transistor-level performance (growing at ~13% CAGR) and the final maximum on-chip frequency required by chip-level microprocessor and ASIC SOC designs.

Therefore, the PIDS intrinsic transistor design model is under evaluation for revision in the 2012 ITRS Update work. It is proposed that a lower 8% intrinsic transistor performance trend would still give adequate "headroom" for designers to create chips at the new lower Design TWG 4%-growth-rate chip-level frequency target, yet not push process manufacturing technology too fast in order to also meet affordability and process control and yield and power requirements. Additional cross-TWG work is required to reach consensus on the scenario that will balance the requirements for reasonable technology progress with design for manufacturability and performance. The progress and final results of the 2012 Update cross-TWG consensus will be reported out at the regional ITRS workshops in 2012.

The delayed work until 2012 will also allow PIDS to model (in the near term with MASTAR static models and in the long term with TCAD dynamic models) the technical specifications that drive Vdd and current target models. The PIDS model work includes additional modeling of a ring-oscillator emulation with a simulated load, which significantly lowers (by about 22×) the frequency characteristics of an individual transistor, but is more representative of what a designer might experience at the chip-level logic design.

In addition, the PIDS work for the 2012 Update will include modeling of the new accelerations (announced recently by leading companies), of the PIDS MugFET and III/V Ge "equivalent scaling" technologies line items – comparing them with performance and power improvements also provided by the Fully Depleted Silicon-on-Insulator (FDSOI) pathway options (refer to the Equivalent Scaling Update special topic; and additional details in the PIDS chapter).

An estimate of the potential impact of the 4-year acceleration of the MugFET technology can be seen in Figure 9 FreqTopic tbd1. Also included are trend lines for a possible 2012 Update scenario of a slowing of the FDSOI trend model to an 8% CAGR; and the scenario of the slowing of the accelerated MugFET timing to 5% CAGR to match the FDSOI trend at the 2026 target. These scenarios are examples to clarify for the reader the possible approaches that might be taken in the 2012 Update work, and do not necessarily represent the final 2012 Update cross-TWG consensus.

The reader should note Figure 10 (a "cartoon overlay" graph of the 2009 and 2011 On-Chip Frequency comparison to the PIDS Intrinsic Frequency). The 2011 PIDS Ring-Oscillator frequency model (meant to give a more realistic representation of the typical on-chip intrinsic device performance) presently uses a 13% average growth trend. The base graph data plot was provided by the Test TWG from historical data the Test TWG gathered and compared to the Design TWG targets in past (2005-2007) and present (2011) ITRS versions.

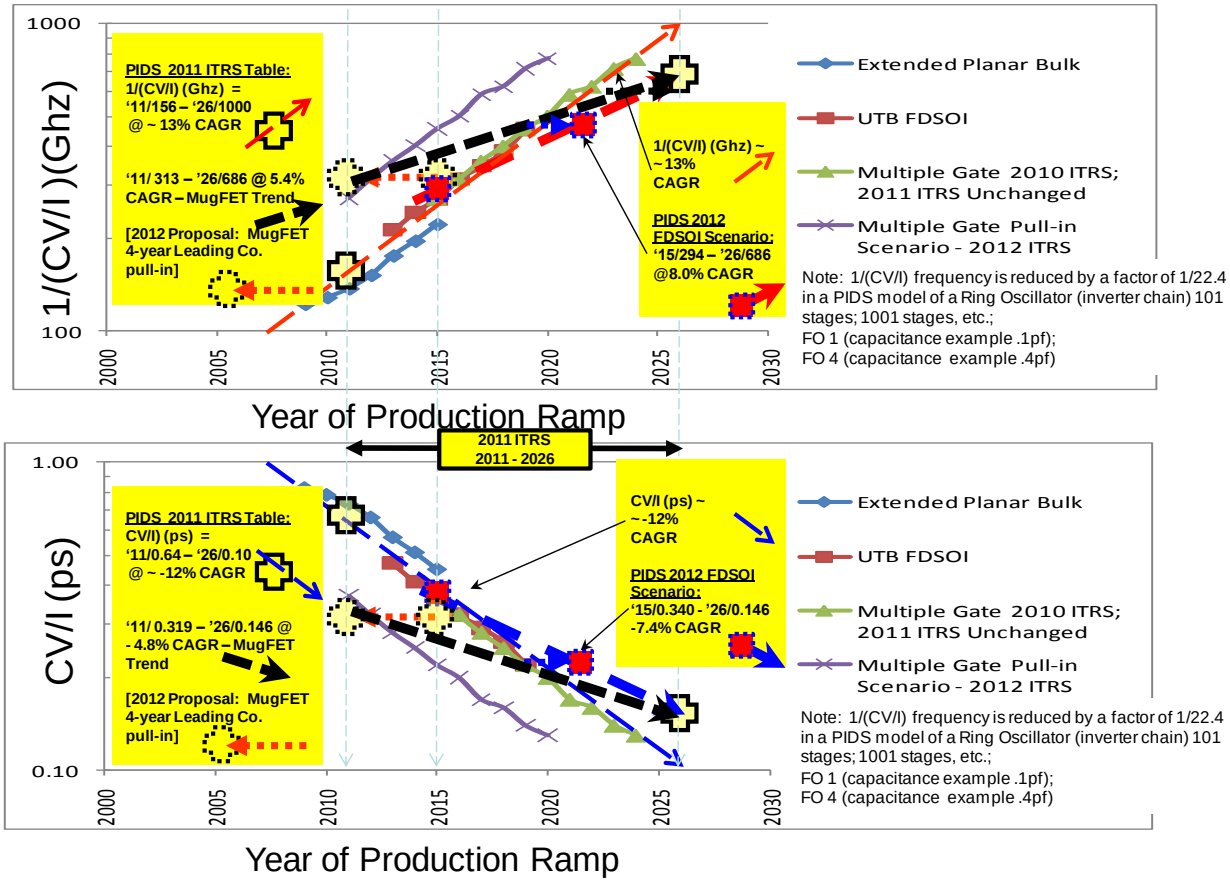


Figure 9 *2012 Update Model Trend versus 2009/2011 ITRS PIDS TWG Transistor Intrinsic Frequency (1/(CV/I)) Performance Trends*

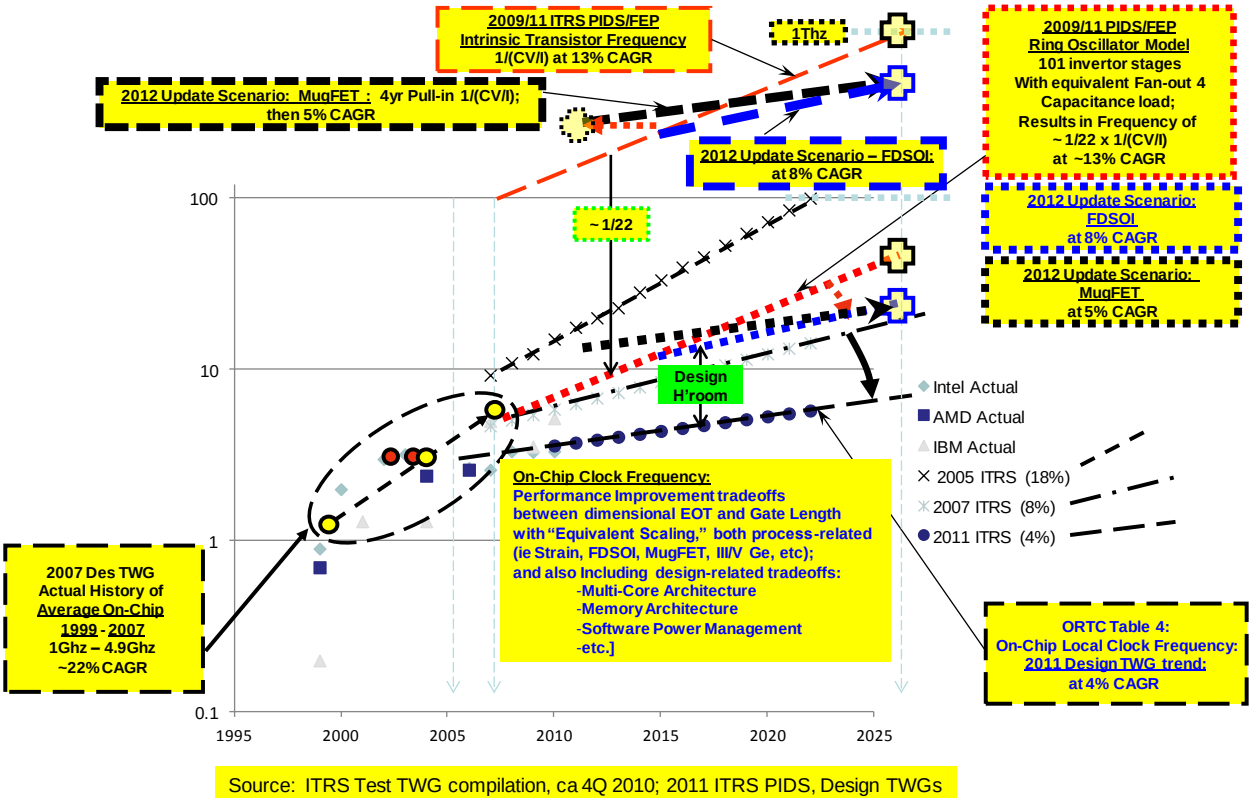


Figure 10 *Design On-Chip Frequency vs. PIDS Intrinsic Transistor and Ring Oscillator Model Frequency*

GRAND CHALLENGES

IN THE NEAR-TERM (THROUGH 2018) AND LONG-TERM (2019 AND BEYOND)

OVERVIEW

The continued research and development efforts in our industry have brought about reacceleration and diversification of scaling. MPU density on a two year cycle till 2013 and three year cycle afterwards. Flash device's scaling continues to sustain a bits/chip doubling per two-year cycle, DRAM bits/chip doubling is on a three-year cycle. The word "node" cannot define technology trend clearly anymore. In the chapter on PIDS, it is observed that there are many choices to improve MOSFET performance, which we call "Parallel Paths" of planar bulk metal-oxide semiconductor field effect transistor (MOSFET), multiple gate field effect transistors (e.g., FinFET), and silicon-on-insulator MOSFET.

The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges in patterning, advanced materials, strain engineering particularly in non-planar device structures, junction leakage, process control, and manufacturability. Challenges also span SoC and SiP integration of CMOS with new types of memory devices. All these will be essential elements for the continuous growth of the semiconductor industry.

Each ITWG identified and listed "Difficult Challenges," which are included in this Executive Summary. In this section of "Grand Challenges," major "Difficult Challenges" are selected and described. This section is intended to help readers grasp an overall picture concerning major technological issues.

These "Grand Challenges" are classified into two categories: "Enhancing Performance" and "Cost-effective Manufacturing." They are also described according to the "near term" (2011 through 2018) and the "long term" (2019 through 2026) timeframes of the Roadmap.

IN THE NEAR TERM (THROUGH ~ 2018)

ENHANCING PERFORMANCE

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

Scaling planar CMOS will face significant challenges. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architectures, in addition to continuous process control improvement are needed to break the scaling barriers.

Reduction of the equivalent gate oxide thickness (EOT) will continue to be a difficult challenge particularly for the HP and LOP segments in the near term despite the inception of high-κ metal gate (HKMG). Interfacial layer scaling and/or silicon-high-κ interface quality are critical to the EOT scaling for the 22 nm node and beyond. Integration of higher-κ materials while limiting the fundamental increase in gate tunneling currents due to band-gap narrowing are also challenges need to be faced in the near term. The complete gate stack material systems need to be optimized together for best device characteristics (power and performance) and cost. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

Planar MOSFET requires high-channel doping to control short-channel effects, the trade-offs are mobility degradation and increased leakage power consumption. Using doping to control threshold voltage in scaled device also causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. New device architecture such as multiple-gate MOSFETs (e.g., finFETs) and ultra-thin body FD-SOI are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The continued research and development efforts in the industry have brought about reacceleration and diversification of scaling. The baseline memories now include both stand-alone and embedded DRAM and SRAM, and both NAND and NOR Flash. The new prototype memories table includes silicon/oxide/nitride/oxide/silicon (SONOS), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change memory (PCM).

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. The need to increase bit density and to lower production cost is driving toward $4F^2$ type cell, which will require high aspect ratio and non-planar FET structures.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash memory has become a new technology driver for both critical dimension scaling, materials and processing (lithography, etching, …) technology ahead of DRAM and logic; . Continued FLASH density improvements in the near term rely on the thickness scaling of two key dielectrics of the memory cell, namely the tunnel oxide and the intergate dielectric, in a way that guarantees the charge retention and endurance requirements; the introduction of high-κ materials will be necessary. 3-D NAND flash is being developed to build high-density NVM beyond 256 Gb. Cost effective implementation of this new technology with MLC and acceptable reliability performance remains a difficult challenge. Non-Volatile memory challenges also include the inception into mainstream manufacturing and the scaling of new memory types and storage concepts such as MRAM, phase-change memory (PCM), and FeRAM, for example. MRAM scalability of cell-size and write-power reduction still needs further breakthroughs. FeRAM critical issues relate to cell endurance, scalability of power supply and cell-size. Another challenge for MRAM and FeRAM going forward is their cost effective integration with logic technologies, FeRAM being particularly more challenging while MRAM seems more suitable for integration in the backend of the flow.

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES -]

Cost, power consumption and performance of wireless transceiver ICs in the <10GHz and the mm-wave applications continue to be the main technology drivers. The <10GHz application space, serviced by deep sub-micron CMOS technologies with emerging high κ dielectrics and channel strain engineering may require techniques to keep the device mismatch and the 1/f noise within acceptable levels. To adopt advanced RFCMOS early, incorporating less expensive integrated passive components as part of a total solution would become a technology trend where innovation would be needed to achieve higher density capacitors. Applications that use HBT devices will benefit from a more aggressive vertical scaling. MEMS development, MEMS integration with active Si and off-chip passive network processes are expected to significantly contribute to the overall system performance. Mm-wave applications will benefit from development of low cost non-Si (GaN) based devices.

Signal isolation between the digital and the analog regions of the chip is becoming more critical as the chip complexity and operating frequencies increase while the power supply voltage decreases. While noise coupling through the power supply and the ground line can be addressed by design techniques, substrate noise coupling reduction may require significant amount of innovation such as KΩ-cm high resistivity substrate.

MEMS

The ITRS MEMS Technology Working Group (TWG) was established is 2011 and tasked to develop a new chapter for the ITRS Roadmap. The MEMS devices considered in here (accelerometers, gyroscopes, microphones, and RF varactors) will generally see a continuous incremental increase in performance with key focus areas being decrease in package size and cost. The greatest challenges for the MEMS technologies are related to their integration and primarily linked to the back-end of manufacturing, packaging and test. As mobile internet device manufacturers work to decrease size and weight, extend battery life, and integrate new functionalities, their pull on MEMS device manufacturers is for smaller package size and integration. The near term challenges include: production of 10 degree-of-freedom (DOF) MEMS inertial measurement units (IMUs), incorporating 3-axis accelerometers, 3-axis gyroscopes, 3-axis magnetometers (compass), and a pressure sensor (altimeter).

NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Reduction of the equivalent gate oxide thickness (EOT) below -0.7 nm with appropriate metal gates remains as the most difficult challenge associated with the future device scaling. Higher dielectric constant dielectrics with adequate conduction and valence band offsets with silicon and thinner interfacial layers are required. Reduction of interface states for gate stack on multi-gate devices is one of key challenges for 16 nm half-pitch and beyond. Another critical challenge is scaling the interfacial layer between the high-κ dielectric and the silicon without channel mobility degradation from increased Coulomb and remote phonon scattering. Higher mobility materials such as SiGe, Ge, and III-V compound semiconductors will be needed for channel transport enhancement which introducing additional challenges for future high-κ dielectric stacks due to the complex nature of their interfaces with channel materials. Furthermore, reliability requirements for newer high-κ oxides, including dielectric breakdown characteristics (hard and soft breakdown), transistor instability (charge trapping, work function stability) must be resolved.

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance requirement to 20-25- fFand reducing the parasitic capacitances in buried bit line or buried word line technologies. Storage cell capacitance requirements resulted in the introduction of dielectric materials with a higher dielectric constant (higher-κ) now in production for DRAM capacitors using metal-insulator-metal (MIM) structures. Besides the high-κ dielectrics and high work function electrode, new technologies for storage node formation with ultra high aspect ratios are needed. Therefore, new oxide etching technology and sidewall cleaning technology for ultra high storage node pose significant challenges and needs to be developed.

Continued FLASH scaling in the near term relies on the thickness of two key dielectrics of the memory cell, namely the tunnel oxide and the intergate dielectric, in a way that guarantees the charge retention and endurance requirements. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. Scaling the tunnel dielectric thickness must simultaneously guarantee good charge retention properties (drive for thicker films) and high write/erase performance (drive thinner films).. The present interpoly dielectric technology is based on oxy-nitride stacked layers and likely not suitable for aggressive reduction of equivalent oxide thickness due to unacceptable charge retention properties. Thus, the introduction of high-κ materials at this step will be necessary. Aside new materials, the structural stability and overall process integration represent critical challenges for the inception of 3D NAND technologies critical to continued effective flash memory density scaling.

32 AND 22 NM HALF PITCH [LITHOGRAPHY]

32 nm half pitch remains a crucial turning point for lithography imaging scheme. The 193 nm water immersion process is limited with NA to resolve this pitch, unless tight pitches are split into larger ones by double patterning or exposure; however the lithography cost will almost double. Extreme-UV lithography (EUVL) with wavelength reduced to 13.5 nm, an order of magnitude smaller than that of the water-immersion wavelength of ArF excimer lasers, is the official hope of the industry to advance Moore's law. EUVL does not need double exposure until approaching the 11 nm half pitch. As a result there is less restriction in design rules. However, EUVL is delayed by the lack of high-power and high-efficiency sources, fast resists, defect-free and high-flatness masks, as well as related infrastructures. Development efforts in these areas are heavy. Multiple-e-beam maskless lithography, which has the potential to bypass mask difficulties, remove restricted design rules, and provide manufacturing flexibility, is in an early-stage of development. Two pre-alpha tools are in the field. Progress has been made in demonstrating high-resolution imaging and CD control. Timing of manufacturing tools, costs, defects, overlay accuracy, and resists are other areas to further develop.

For 22-nm half-pitch lithography, water-immersion 193 nm scanners with spacer lithography or multiple patterning will be applied to overcome the single patterning limitation, but with extremely large mask error enhancement factor (MEEF), wafer line edge roughness (LER), and design rule restrictions. Resorting to more than two passes through the patterning tools can alleviate some of the above problems at the expense of higher costs. The numerical aperture of EUV systems will have to be raised to more than 0.36 to have the k_1 factor comparable to NA 0.25 for 32 nm half pitch. There is a likelihood of increasing the number of mirrors in the imaging lens, thus leading to requirement of even higher power source while limiting throughput loss, thus less favorable economy. Multiple-e-beam maskless lithography will be better developed by that time but it has to support a high writing rate per beam or more parallelism to maintain the increased pixel count within the same-size field. If the potential is realized to keep the per-pass exposure and processing cost as well as the footprint similar to that of mask-based exposure tools, then it will be the most economical and sought-after solution for logic and memory applications.

MASKS [LITHOGRAPHY]

The mask technology is becoming very expensive and challenging. Mask cost has escalated each generation. Increased resolution plus larger MEEF, due to higher levels of resolution enhancement technique (RET), make the mask CDU difficult to meet. Double and multiple patterning impose stringent requirement of mask pattern placement accuracy. Mask feature sizes becoming sub-resolution coupled with finite absorber thickness and polarized illumination worsen the problem. EUV masks have further stringent requirements of defect-free ultra-flat substrate and exposure without a pellicle. Inspecting advanced masks is expensive and time consuming. The inspection resolution is reaching limits with practical inspection wavelengths. Actinic mask inspection and verification are eventually inevitable for EUVL. It further adds to the cost and complexity of the EUV mask infrastructure.

RESISTS [LITHOGRAPHY]

LER of photoresist has substantially sustained the same absolute value and therefore has attained an even larger percentage of CD. As pattern geometry shrinks, shot noise starts to become an issue. Resist collapse after development limits its height-to-width aspect ratio to between 2.5 and 3, thus reducing the absolute resist thickness at each technology-generation advancement. With immersion lithography, resist material development has to ensure low resist-induced defectivity, further restricting material choices. For EUVL, resist outgassing can contaminate the delicate reflecting optical surfaces. The tradeoffs between high resist sensitivity for throughput, low resist sensitivity for shot noise, and low LER, impose more problems than just resist collapse. E-beam resists also have to trade off for sensitivity and shot noise as well as LER. The sensitivity requirement is not as severe as that of EUVL.

CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. In particular, resist slimming and profile-control of the sidewall, which are commonly utilized to minimize the dimension of effective gate length (L_{eff}), have made CD control far more difficult. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. The inception of increasingly restrictive design rules aimed to promote design regularity have become mainstream as key enablers for near term scalable CD control. Line-edge-roughness (LER) has become also a critical element of device variability. Suppression of LER will continue to pose significant challenges to patterning processes (etch and lithography) as well to metrology in terms of accuracy and throughput. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, the industry introduced high-conductivity metal and low-permittivity dielectric through damascene processes at 130 nm logic technology M1 half-pitch. Even lower permittivity dielectric has been introduced at 45 nm half-pitch. The continued scaled-down interconnect poses increasing challenges to technology development and manufacturing. The fast introduction of new metal/dielectric systems becomes critical. For low-κ dielectrics, the conventional approach is the introduction of homogeneous porous low-κ material. Reduction of κ damage due to Etch and CMP processes becomes more important with more porous materials. Another approach is air gap. It attracted attention because it keeps same low-κ materials with more volume of air gaps that gives lower effective κ. Among various techniques to incorporate air gaps, thermal or UV degradable sacrificial layer method is one of the low-cost approaches. Furthermore, low-κ material must have sufficient mechanical strength to survive dicing, packaging, and assembling. For the metal, fast rising resistivity of narrow Cu wires due to electron scattering at the Cu/barrier metal or dielectric interfaces and the grain boundary has become a key challenge. A very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability.

ENGINEERING MANUFACTURABLE INTERCONNECT [INTERCONNECT]

The integration of conductive and low-κ material must meet material, geometrical, planarity, and electrical requirements. The low-κ material with good mechanical, chemical, thermal, and physical properties are needed for manufacturable integration with other processes that may induce damage, in particular dry and wet etching, ashing, sputtering, and polishing. Defect, variability, and cost must be engineered to ensure a manufacturable process. The advancement of interconnect should address performance, power, and reliability issues for traditional scaling or equivalent scaling with functional diversity. Since material solutions with traditional scaling cannot deliver performance, new technology has been proposed in recent years including 3D (including tight pitch through silicon vias (TSV)) or air gap structures,

different signaling methods, novel design and package options, emerging interconnect using different physics and radical solutions, etc. The realization of these innovative technologies challenges new material systems, process integration, CMOS compatibility, metrology, predictive modeling, and optimization tools for interconnect/packaging architecture design.

POWER MANAGEMENT [DESIGN]

Cost-effective heat removal from packaged chips remains almost flat in the foreseeable future. Driven by the 2× increase in transistor count per generation, power management is now the primary issue across most application segments. Power management challenges need to be addressed across multiple levels, especially system, design, and process technology. Circuit techniques to contain system active and leakage power include multiple V_{dd} domains, clock distribution optimization, frequency stepping, interconnect architectures, multiple V_t devices, well biasing, block shutdowns among others. The implementation challenges of these approaches expand upwards into system design requirements, the continuous improvements in CAD design tools for power optimization (including design robustness against process variability), and downwards into leakage and performance requirements of new device architectures.

CIRCUIT ELEMENT AND SYSTEM MODELING FOR HIGH FREQUENCY (UP TO 160 GHZ) APPLICATIONS

Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-, CMOS-, and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

FRONT-END PROCESS MODELING FOR NANOMETER STRUCTURES [MODELING AND SIMULATION]

Advanced USJ formation is critical to support continued scaling of device features. Definition of drain extension using millisecond anneal, SPER, as well as by in situ doped epitaxial layers, are expected to be widely used to reduce junction depth, sharpen junction gradient, and enhance activation. More physical models are needed to capture point and extended defects, dopant, and co-dopant evolution and interactions, during non-equilibrium transient process of millisecond anneal. Modeling capabilities need to be enhanced or developed to capture crystal/amorphous growth front evolution and defect generation during SPER. New models are needed to properly capture initial doping states created by various in situ epitaxial processes. Process modeling available for bulk silicon substrate will need to be adapted or extended to various Si-based substrate including SiGe:C, Ge, SOI, epilayers, and ultra-thin silicon on insulator, as well as high mobility compound materials such as GaAs, InGaAs etc. Additional factors, including, possible anisotropy, interface/surface type effects, and intrinsic strain effects, need to be take into account. Modeling of advanced implant technologies such as, use of molecular species, non-beam line implant, and cooled or heated substrate, will be needed. Epitaxial processes such as SiGe:C will be expanded to multi-channel devices with complex geometries, therefore, modeling of epitaxially grown layers including the shape, morphology and defect generation will be critical to optimize such epitaxial processes. Extensive use of stress to enhance device mobility will continue. More accurate modeling of stress including material properties evolution during process such as plastic deformation during anneal, and stress relaxation due to defect generation will be needed. There will be continued needs for refining metrology / reverse modeling of USJ - 2D/3D doping/stress profiling to sufficient resolution to help calibration of simulation models and parameters. Devices are expected to largely deviate from quansi-2D and become 3D in nature, therefore more advanced 3D meshing, and parallel processing to improve 3D computational efficiency and accuracy will be needed. Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces will be helpful in understanding nano-scale feature related effects. High-κ/metal gate is expected to be the basic building block, therefore modeling of High-κ/metal gate work function, interfacial atomic structures and their influences on mobility and reliability, will be necessary.

COST-EFFECTIVE MANUFACTURING

DESIGN PRODUCTIVITY AND DESIGN FOR MANUFACTURING [DESIGN]

The number of available transistors doubles every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and IP reuse are key considerations for this issue. Challenges at high-level abstraction, platform-based design, multiprocessor programmability, design verification, analog and mixed-signal circuit synthesis are critical to secure design productivity scaling at a pace consistent with process technology cycles. Cost-effective product manufacturing also requires continuous improvements in the area of design for manufacturability, specifically areas such as design to minimize performance/power variability, lithography-friendly designs (regular layout styles consistent with increasingly more restrictive design rules), and design for testability and reliability.

TEST COMPLEXITY [TEST AND TEST EQUIPMENT]

The complexity of next generation testing technologies is further convoluted by design and process interaction of heterogeneous integration in one device such as 3DIC, which imposed challenges in yield learning for production ramp. The device characteristics of heterogeneous integration will not only be dependent on layout environment also will be relative to integration of process procedure and the functionalities of design modeling. The effectiveness and efficiency of test and analysis of product failure becomes the gating factor for yield ramp. The intelligent test data mining feedback tests data in order to tune manufacturing and device's traceability (of which for each manufacturing process becomes increasingly important). The areas for further improvement include new test equipment, test methodology, and design software for effective defect localization, thermal effect of physical failure analysis techniques, and efficient implementation of refined DFM solution for heterogeneous integration devices.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law may not translate to test naturally. The new test requirements for increasingly complex devices drive innovative new testing technology to continue economic scaling of test cost (such as DFT, concurrent testing, adaptive test and built-in testing— self-test, self-diagnostic, self-repair, self-calibration, self-compensation.) of which have enabled higher levels of test parallelism very successfully in keeping test costs in check to date and near term. In the opposite cost-direction, test tooling costs, including probe cards, are not scaling and threaten to dominate the total test cost if present trends continue. Accelerating the test learning curve for new device architectures or integration schemes is critical to maintain test cost scaling curve in sync with overall technology cost-scaling goals. Product cost optimization should strike a balance between design, manufacturing, yield learning, and test while securing overall quality of shipped products. The intelligent test data mining with dynamic test flow, convergence of test and system reliability solutions, integration of simulation and modeling of test interfaces hardware and instrumentation into the device design process are challenging opportunities for test cost scaling reduction.

RESPONDING TO RAPIDLY CHANGING COMPLEX BUSINESS REQUIREMENTS [FACTORY INTEGRATION]

Wide ranging business models beyond the integrated device manufacturer (IDM) such as the fabless and foundry model, joint venture, and the variety of task sharing and out-sourcing scenarios have become pervasive in response to customers' rapidly changing complex business requirements. Furthermore, diversified customers' requirement such as non-incremental technology introductions, complex product designs and large-scale transistor integration, and process complexity have placed strong demand on manufacturing environments to rapidly and efficiently adapt to high-mix and low-volume product runs. These requirements continue to pose critical near-term challenges in several areas such as integration of larger numbers and different types of equipment, software applications, and fully featured software systems to manage the factory complexity while enabling decreasing time to ramp high volume production.

Development of information exchange/control platform covering all the relevant operation fields, extending from design, mask, front-end-of-line (FEOL), and back-end-of-line (BEOL) to testing, packaging, etc., is also a crucial challenge. Continuous improvements to model factory capacity and performance to optimize output, improve cycle time, and reduce cost are key to successful high-mix factory operations.

IMPROVEMENT IN TRADE-OFF BETWEEN MANUFACTURING COST AND CYCLE TIME [FACTORY INTEGRATION]

Enhanced tool availability and productivity, improvements in material handling automation and systems for operational flexibility and control; single-wafer manufacturing and wafer level data; and the reduction/elimination of both utilities and non product wafers (NPW) consumption; are representative areas for continuous improvement in 300 mm lines to

meet the challenges of cycle time and cost reduction. The transition from 300 mm to the next wafer size (i.e., 450 mm) is another critical challenge for the semiconductor industry in the 2014–2016 time frame. This transition is considered critical to simultaneously meet the 30% cost/die reduction and a 50% improvement in cycle time.

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

The challenges for assembly and packaging include concerning 3D IC chip stacking:

- Con-current Design & Environment

  Without sacrificing performance, cost or cycle time, 3D IC design demands a shift from traditional package design methods, tools and environment to a system design approach – also known as chip-package-system co-design. Some of new complications include the following:

  - Comprehending the interaction and IO planning of multiple functions on a single chip and package
  - Handling of an order of magnitude more design data
  - Minor tweaks in the IC or package design can lead to additional levels of design work
  - The need for tighter integration of chip IO planning, system-level reliability and manufacturability testing, as well as system-level electrical, thermal and mechanical modeling add reliability here as well
  - The learning curve associated with using new, more powerful package design tools
  - Cost and time-to-market trade-offs

Besides, challenges for 3D IC also include:

- Materials: Substrate, Interposer, Low K Dielectric Compatible Materials, Integrated Passives and Underfill.
- Process: Stacking, Bonding (CoC/CoW/WoW), Wafer Thinning, Thin Wafer Handling, TSV, Re-work and Self-assembly.
- Testing: Access, Cost and KGD.

SOLUTIONS FOR INTEGRATION OF OFF-CHIP COMPONENTS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES, ASSEMBLY AND PACKAGING]

System-in-package solutions have been developed to meet different applications and system requirements especially in the rapidly changing and increasing market of portable wireless communication devices. The integration of these SiP solutions to construct a universal design platform is increasingly important. High Q RF devices by MEMS or other processes are usually off-chip and need to be made as integrated passive devices (IPD). Three-dimensional stacking and embedded components are two major methodologies to address off-chip components. Forming passive component (as opposed to inserting discrete components) into substrates often involves additional materials such as high-κ dielectric for capacitors, resistive films or paste for resistors, and high permeability (μ) material for inductors. Devising process simplification for this variety of embedded passives is a key challenge to enable a cost-effective alternative. Testing and tuning also pose significant challenges, especially after packaging or assembly processes. Accurate models that include process tolerances as well as circuit and tester parasitic elements are needed for designers to simulate circuit performance with embedded passives before the manufacturing process. Lack of CAD tools for embedded passives also needs to be resolved.

CHEMICAL AND MATERIAL ASSESSMENTS [ESH]

The rapid introduction of new chemicals, materials, and processes requires new rapid assessment methodologies to ensure that new chemicals and materials can be utilized in manufacturing without inducing new hazardous impacts on human health, safety, and the environment. Although methodologies are needed to meet the evaluation and quantification demands for ESH impacts, the focus is currently on expediting process implementation. As such, near-term challenges - include emissions reduction from processes using chemicals classified as having significant global warming potential (GWP), the complete transition to lead-free packaging, biotoxicity and the need for a robust and rapid assessment of new materials/chemicals critical to surmount technology roadblocks while complying with ESH requirements

RESOURCE CONSERVATION [ESH]

As the industry grows and its technology advances toward finer patterning and larger wafer sizes, the natural tendency is toward increased use of water, energy, chemicals, and materials. Resource conservation is becoming a major concern with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. Thus, it is necessary to develop diverse process equipment capable of utilizing resources efficiently. Continuous improvement is needed in

chemicals and materials utilization and energy, water consumption reduction in facilities and processing equipment, as well as in efficient thermal management of clean rooms. 450 mm process tool development is an opportunity and a "must" of breakthrough.

DETECTION OF MULTIPLE KILLER DEFECTS AND SIGNAL-TO-NOISE RATIO [YIELD ENHANCEMENT]

Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Inspection sensitivity can be increased to address defect size trends; however challenges arise in terms of efficiently and cost-effectively differentiating defects of interest (DOI) from a vast amount of nuisance and false defects. Reduction of background noise from detection units and samples are key challenges to enhance signal to noise ratio for defect delineation. Increasing aspect ratios and interconnect complexity will continue to pose increasingly difficult challenges and also opportunities to inspection tools development.

LAYOUT STYLE AND SYSTEMATIC YIELD LOSS: HIGH THROUGHPUT LOGIC DIAGNOSIS CAPABILITY [YIELD ENHANCEMENT]

Random logic areas are very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Solutions exist but need continuous improvements. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows accommodation; ATE architecture that lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

WAFER EDGE AND BEVEL CONTROL AND INSPECTION [YIELD ENHANCEMENT]

Defects and process problems around wafer edge and wafer bevel are known to cause yield problems. Development and continuous improvement in terms of defect detection, throughput, and cost of ownership (CoO) of wafer edge and bevel defect inspection tools are increasingly critical to yield enhancement in advance device technologies.

FACTORY-LEVEL AND COMPANY-WIDE METROLOGY INTEGRATION [METROLOGY]

Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). *In situ* and inline metrology has become requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into an efficient database for determining process control parameters and key correlations to drive yield enhancement. Such efficient and seamless integration requires that standards for process controllers and interfaces, data management and the database structure be established. Continuous improvement of sensors, including calibration, sensing method, and data processing is clearly expected. Development of new sensors must also be concurrently done with the development of advanced process modules and ever increasing aspect-ratio levels

MEASUREMENT OF COMPLEX MATERIAL STACKS, INTERFACIAL PROPERTIES, AND STRUCTURES [METROLOGY]

Metal-gate high-κ gate stacks, advanced strain and mobility enhancement techniques, as well as advanced interconnect and low-κ dielectric structures require novel or continuous improvement of measurement methodologies and standards in terms of critical dimensions (film thickness, feature sizes, LER, etc.), materials' physical properties (e.g., strain), and electrical properties including interface characteristics (e.g., workfunction, interface states, etc.). Metrology of film stacks for both front-end and back-end generally provide average physical or electrical property behavior from large area test structures. Therefore, new metrology techniques capable of characterizing stack structures at near nominal dimensions are also needed in the near term.

CRITICAL METROLOGY CONSIDERATION—PRECISION AND UNCERTAINTY [METROLOGY]

When comparing measurements with numbers in the roadmap, there are several important considerations. The validity of the comparison is strongly dependent upon how well those comparisons are made. The conventional interpretation of the ITRS precision has been in terms of the single tool reproducibility. The term "precision" is best understood in broader terms as *uncertainty*. Measurement error is a complex function of time (reproducibility), tool (tool-to-tool matching) and sample (sample-to-sample bias variation). The measurement uncertainty is thus defined by the total bias variation with measurement-to-measurement, tool-to-tool, and sample-to-sample components. These components may be of varying importance depending on the instrument and the application.

LITHOGRAPHY METROLOGY [METROLOGY]

Lithography metrology continues to be challenged by rapid advancement of patterning technology. A proper control of the variation in transistor gate length starts with mask metrology. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. The metrology needs for process control and product disposition continue to drive improvements in precision, relative accuracy, and matching. Acceleration of research and development activities for CD and overlay are essential if to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability which is another important metrology challenge.

IN THE LONG TERM (2019 THROUGH 2026)

ENHANCING PERFORMANCE

MANAGEMENT OF LEAKAGE POWER CONSUMPTION [DESIGN]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness, and threshold voltage. This presents severe challenges in light of both technology scaling and variability. Off-currents in low-power devices increase by a factor of 10 per generation, and will emphasize a combination of drain and gate leakage components. Therefore design technology must be the key contributor to maintain constant or at least manageable static power.

IMPLEMENTATION OF NON-CLASSICAL CMOS CHANNEL MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND EMERGING RESEARCH DEVICES]

To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, high transport channel materials such as III-V or germanium thin channels on silicon, or even semiconductor nanowires, carbon nanotubes, graphene or others may be needed. Non-classical CMOS devices need to be integrated physically or functionally onto a CMOS platform. Such integration requires epitaxial growth of foreign semiconductor on Si substrate which is challenging. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development

IDENTIFICATION, SELECTION, AND IMPLEMENTATION OF NEW MEMORY STRUCTURES [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

Line-dense, fast, and low-operating-voltage non-volatile memory will become highly desirable, and ultimate density scaling may require three-dimensional architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance. Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness (EOT) and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or developing alternative emerging technologies.

FUTURE CHALLENGES OF RF AND AMS CMOS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES]

Radio frequency and analog/mixed-signal (RF and AMS) CMOS technologies are based upon the CMOS devices of the Process Integration, Devices, and Structures (PIDS) chapter utilizing the low standby power (LSTP) roadmap for microwave applications and the high performance (HP) roadmap for millimeter-wave applications. As reflected in the HP & LSTP roadmaps, fundamental changes in device structures such as the introduction of multiple-gates and/or fully-depleted SOI will be required to sustain continued performance and density improvement. The electrical characteristics of these devices are fundamentally different from those of conventional CMOS. Potential benefits include higher voltage-gain and lower coupling between the drain and body. But these differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries. Thus, the fabrication of conventional precision analog/RF driver devices to be integrated alongside the scaled CMOS devices may require separate process steps. Even now, the impetus to enable system-on-chip (SOC) applications

is encouraging the incorporation of optional analog or high-voltage devices and thereby expands the menu of potential devices albeit with the attendant cost increases.

FIGURES OF MERIT (FOM) FOR RF AND AMS DEVICES [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES]

This 2011 RF and AMS Chapter presented Figures of Merit (FoM) for RF and AMS CMOS, Silicon bipolar and BiCMOS, Compound Semiconductors consisting of elements from groups III and V, Passive On-Chip Devices, and High Voltage MOS. Extracting reliable figures of merit (FoMs) from high frequency measurements become more difficult as device performance levels increase and parasitic resistances and capacitances are reduced. For this reason a sufficient device area with regards to transistor layout is recommended to get capacitances exceeding 20 fF, which is a lower limit for reliable data. Measurement, de-embedding, and parameter extraction methodologies can have a significant impact on RF FoM. Although some complex procedures are developed to obtain the accuracy required for compact modeling, most companies utilize similar basic techniques to measure and monitor device cut-off frequencies (f_T), especially for high-speed wired-communication devices.. In addition, self resonant frequency (SRN/fmax) is also a very important device parameter especially for wireless communication devices such as low-noise-amplifier (LNA). The fmax, however, strongly depends on the layout pattern including power/ground lines. Standardization of the transistor pattern for fmax extraction might be discussed to make roadmaps on f_T and fmax. The discussions about FoM will require the sophisticated and commonly authorized evaluation procedures.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Line edge roughness, trench depth and profile, via sidewall roughness, etch bias, thinning due to cleaning, CMP effects, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge. Etching, cleaning, and filling high aspect ratio structures, especially low-κ dual damascene metal structures and DRAM at nano-dimensions are also big challenges. Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermo-mechanical effects. Novel/active devices may be incorporated into the interconnect lines. Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets is a key challenge.

RESIST MATERIALS [LITHOGRAPHY]

Limits of chemically amplified resist sensitivity come after 22 nm half pitch due to acid diffusion length. With aggressive scaling of devices, the required gate CD control comes down to 1.3 nm in 3σ with a line width reduction (LWR) of less than 1.3 nm in 3σ in 2018 for every lithography potential solution. (Please note that Si-Si lattice distance is 0.235 nm.) New resist materials with improved dimensional, LWR control and low defect density in less than 10 nm size are necessary. Resist and antireflection coating materials composed of alternatives to PFAS compounds are expected for future ESH concern.

TRANSITION TO NOVEL STRUCTURES FOR BOTH CMOS AND MEMORY DEVICES [FRONT END PROCESSES]

Several scenarios coexist for keeping continued scaling of CMOS and memory devices. It is anticipated to proceed with scaling (equivalent scaling), by introducing new materials, new structures, and/or 3D integration. Among all, the selection of a fundamental structure for CMOS is very challenging, for example, a channel material and a multi-gate structure will require new process technologies to be concurrently developed. These technologies include starting materials, surface preparation, lithography, pattern etching, and gate stack with booster technique, doping, metrology, process uniformity, and reliability. Once selected, there is no going back. Coordination and discussion are needed in all aspects among ITWGs viewed from process integration and manufacturing. In the memory area, charge-based devices are facing physical limits such as variability and cross-talk. In order to maintain scaling trends in both cost and functionality, innovative technologies will be needed by realizing new data-storage mechanisms or cost-effective 3D integration.

NON-DESTRUCTIVE, PRODUCTION WORTHY WAFER AND MASK-LEVEL MICROSCOPY [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement including physical feature

measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. The combination of high-resolution optics, waveform analysis, and non-charging technique enables precise grasp of 3D structures for CD measurement including sidewall shape and trench structures of damascene process. At the same time, CD metrology tool must be calibrated by using standard reference material or structure for reliable and stable measurement.

POWER AND BANDWIDTH DESIGN IN 3D SCALING [ASSEMBLY AND PACKAGING]

Power delivery and thermal dissipation design in ever extending 3D scaling are indispensible for further system integration. Co-design, low loss dielectrics material and optical signal acceptance at package level are required to extend physical density of bandwidth for digital electronics. Replacing solder balls of flip-chip with low profile fine-pitch Cu posts and introduction of fragile low-k layer in a die would induce critical chip-package-interference. Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult.

MATERIALS TECHNOLOGIES [EMERGING RESEARCH MATERIALS]

There are many challenges to define, prioritize, and reach consensus to recommend potential solutions that will deliver materials with controlled properties. These properties must be defined in sufficient detail to enable ultimately to transfer to the Process and Integrated Device Structures (PIDS) and the Front End Processes (FEP) teams in a timely fashion for further pragmatic research and development. These properties must be able to describe the operation of emerging research devices in high density at the necessary nanometer scale of the long-range roadmap timing horizon and beyond. In order to improve control of material properties for high density devices, research on materials synthesis must be coordinated and integrated in parallel with work on new and improved metrology and modeling. Metrology to characterize properties in a realistic device has an increased need for further development of integrated devices. Accurate multiscale simulation is required for prediction of the device performance. Furthermore, life cycle assessment and risk management of emerging materials become more essential both for business considerations and the sustainability of enterprises.

DEVICE TECHNOLOGIES [EMERGING RESEARCH DEVICES]

Long-term challenges for emerging research devices are divided into those related to memory technologies, those related to information processing or logic devices, and those related to heterogeneous integration of multi-functional components. New memory technologies that combine the best features of current memories are required in a fabrication technology compatible with CMOS process flow. A new manufacturable "beyond-CMOS" information processing technology compatible with a new system architecture is required. Implementation of new information carrier (state variables) other than charges is demanded. A non-binary data representation and non-Boolean logic may be required.

POST-CONVENTIONAL CMOS MANUFACTURING UNCERTAINTY TECHNOLOGIES [FACTORY INTEGRATION]

Uncertainty of novel device types replacing conventional CMOS, and the impact of their manufacturing requirements, will have a big influence on a factory design. Due to the timing uncertainty of the industry to identify and develop new devices, and to create new evolutionary and disruptive process technologies, there is a need to model and design next-generation factories for a wide spectrum of flexibility. Such future factories must have the ability and flexibility to be implemented through early development phases and into production just in time for low risk industry transitions; and also taking into account the potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and with cost efficiency. These are huge industry challenges to simply imagine and define and also for the Factory Integration resources to implement.

COST-EFFECTIVE MANUFACTURING

MODELING OF CHEMICAL, THERMOMECHANICAL, AND ELECTRICAL PROPERTIES OF NEW MATERIALS [MODELING AND SIMULATION]

Increasingly new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists, and furthermore for Emerging Research Devices (see the ERD and the ERM chapters). In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Especially, computational material science tools need to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations. Furthermore, modeling must assist metrology to enable the characterization of novel materials and devices.

IN-LINE DEFECT CHARACTERIZATION AND ANALYSIS [YIELD ENHANCEMENT]

Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

COST CONTROL AND RETURN ON INVESTMENT [LITHOGRAPHY]

Extending lithography to beyond 22 nm half pitch requires the introduction of new lithography technologies such as Extended-Ultraviolet Lithography (EUVL) or new techniques such as multiple patterning or a combination of both. All of these techniques introduce large changes into the single exposure immersion lithography process, targeted presently for the 32 nm Flash Poly uncontacted half-pitch and the 45 nm DRAM contacted M1 half pitch technology cycle. A spacer double patterning is used for 32 nm and 22 nm Flash memories. Therefore, achieving constant/improved ratio of exposure-related tool cost to throughput might be an insoluble dilemma. Mask costs are a significant component of lithography costs even up to high mask usage, so development of cost-effective post-optical masks is necessary. Also cost effective lithography systems are expected for the upcoming 450 mm wafer generation manufacturing.

TEST DEVELOPMENT AS A GATE TO VOLUME PRODUCTION [TEST AND TEST EQUIPMENT]

The increasing trend of functional divergence in a device results in the corresponding complexity of test for yield learning as well as that of test development. Also with the increasing reduction in feature (and defect) sizes well below optical wavelengths, the rapidly increasing failure analysis throughput time, the reduction in failure analysis efficacy, and the approaching practical physical limit to other physical techniques (PICA, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of Design-for-Test (DFT) and test-enabled diagnostics and yield learning become paramount. As the result, yield learning methods need to be augmented with more universal deployment of on-die circuitry (DFT, etc.) across and throughout products, as well as with improvements of the on-die circuitry itself and diagnostic software tools with respect to fault isolation specificity. Where it may have been sufficient to isolate the failing bit in an array or the failing gate in logic in the past, there is a real business need to enable isolating electrically the failing transistor or interconnect , or the semiconductor industry would suffer the economic consequences of reduced yield improvement learning rates on new process technologies.

SUSTAINABILITY AND PRODUCT STEWARDSHIP [ESH]

Business considerations and also sustainability metrics (in a cost-effective and timely way) are required for product stewardship. In addition, Design for Environment, Safety, and Health (DFESH) should become an integral part of the facility, equipment, and product design as well as management's decision-making. Environmentally friendly end-of-life reuse/recycle/reclaim of facilities, manufacturing equipment, and industry products are increasingly important to serve both business and ESH needs.

MEETING THE FLEXIBILITY, EXTENDIBILITY, AND SCALABILITY NEEDS OF A COST-EFFECTIVE, LEADING-EDGE FACTORY [FACTORY INTEGRATION]

Ability to load the fab within manageable range under changeable market demand and to utilize task sharing opportunities such as manufacturing outsourcing is required to keep the manufacturing profitable. Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing continues to challenge. Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] promotes reuse of building, production and support equipment, and factory information and control systems across multiple technology generations. Cost and task sharing scheme is highly expected on industry standardization activity for industry infrastructure development such as data standardization and visualization methodology.

WHAT IS NEW FOR 2011— THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS AND DESIGN

The 2011 revisions of the ITRS Design and System Drivers chapters contain the following key messages and updates.

In the near term, the grand challenges for design technology remain (1) power management, and (2) design productivity and design for manufacturability. Design productivity continues as a central focus of our design technology roadmap, as the economics of scaling depend fundamentally on the ability to deliver new electronic products to the market with low risk and within ever-shorter product cycles. In light of process variability and circuit reliability, design productivity is inextricably coupled with the need for improved design for manufacturability in late-CMOS technology nodes. At the same time, power consumption has become the key technical parameter that controls feasible semiconductor scaling: device roadmaps are now power-driven, and operating frequencies have flattened in several key market domains. Power management is now such a dominant concern in electronic products that a new low power design technology roadmap is now included in the ITRS Design chapter. Additionally, More-Than-Moore continues as a necessary component of semiconductor product scaling. Finally, heterogeneous system and product drivers, including explicitly RF and analog/mixed-signal building blocks, require more attention in the ITRS roadmap.

In the long term, the grand challenges for design technology have been updated as (1) design of concurrent software, and (2) design for reliability and resilience. In the system-on-chip era, the hardware and software "fabrics" are equally important to design success; this is seen in the Design Cost model and in projected future design productivity and low-power design technology improvements. As the scaling roadmap imposes ever-smaller dimensions and pitches, and ever-larger numbers of functions per chip, system resilience to variation, wearout and failure mechanisms will become paramount.

Details of the 2011 revisions and planned 2012 updates for the ITRS Design and System Drivers chapters include the following highlights.

- **Design Chapter**. In 2011, in addition to the first-ever low power design technology roadmap, we provide updates of 3D/TSV design enablement beyond logic-circuit-physical (L/C/P) design, addition of SRAM and resilience to the DFM section, and various updates to the Design for Test, Verification, L/C/P sections. In 2012 we plan to include a more complete More-Than-Moore design technology roadmap.
- **System Drivers Chapter**. New in 2011 are a continuation of the MPU frequency roadmap revision, an update of AMS/RF and Embedded Memory drivers, and an update of SOC-CP and SOC-CS models. A notable planned future update is the addition of an AMS/RF sub-driver (including both System-on-Chip and System-in-Package options), as part of More-Than-Moore roadmapping.

In its interactions with other ITRS technology working groups, the Design ITWG in 2011 focused on roadmap implications of slowing device CV/I improvement, new power-aware roadmaps of the main logic device families in the overall roadmap, and a broad range of 3D integration issues that affect design, assembly and packaging, interconnect, test, and front-end processing technologies. Cooperation with other groups is reflected throughout the two chapters. Additionally, input from the 2nd ITRS-driven EDA Roadmap Workshop at the 2010 ACM/IEEE/EDAC Design Automation Conference, and from the 2011 IEEE CANDE Workshop, is being incorporated.

The take-away for 2011: While power is now at the core of the design roadmap, and will continue to be a major concern in the next decade, other challenges such as design technology for More-Than-Moore, concurrent software, and system resilience and reliability will be key focus areas in upcoming years.

TEST AND TEST EQUIPMENT

2011 TEST ROADMAP

The 2011 edition of the Test Roadmap contains some significant changes to many of yearly revised trends. In addition, the 2011 Chapter includes a new section on 3D/TSV testing that addresses the design and test considerations of this evolving technology. The Cost of Test section has been updated with the results of a survey on Cost of Test. The SOC/DFT and Logic sections also have been significantly reworked to improve synergy and reflect the effects of varying types of DFT.

DEVICE TRENDS

Identification of changes to the major device driver is necessary prior to revising the test roadmap. Fault tolerant devices and architectures were added as drivers for 2011. If a component or system can itself correct or adapt to errors, then errors can be hidden from testing and defect monitoring process, which could then result in a lack of understanding of the quality of the manufacturing process.

COST OF TEST

The Cost of Test section shares the results of a 2011 industry survey on perceived cost drivers. Test cost is an ever increasing concern for the test community. While there have been many efforts to confront the rise in test cost, the reality is that increasing complexity is driving increased cost of test. Improving utilization has been added to near term drivers for test cost.

3D/TSV & DFT

With roll-out of 3D devices (stacked die with TSV and the older SiP devices) the challenges for the test community are rising to a new level. The future will require a focus on an efficient test approach which will simultaneously confirm the proper functioning for multiple interconnected devices within an environment which will likely include multiple technologies and vendors.

The logic and SoC chapter sections and tables sections have been revised this year to better reflect a common DFT theme. Comparisons of various test data methodologies show that there can be a substantial reduction in test data volume, test cost, and test time by choosing the proper data compression technique when designing a product.

ADAPTIVE TEST

Adaptive test was added to the test roadmap in 2009 and has been substantially revised for 2011. The use of real time or previous manufacturing information can improve product yield and reduce cost, but adds the complexity of requiring a reliable per step manufacturing and test information tracking system. The incremental resources may intuitively seem to increase overall product cost, but actual use been shown to result in an overall lower product cost because of the ability to reduce or remove tests that are found to be superfluous.

LOOKING TO 2012

In a quickly changing environment, there are many areas that may have an effect on future roadmaps. 3D devices are currently in their infancy and are expected to be on a learning curve which will impact the roadmap as manufacturing and architectural issues become clearer. Analog and RF will continue to evolve in requirements forcing new test methods and further development in analog DFT. Chip to chip interfaces will drive increases in bandwidth and photonics will need to be comprehended in the roadmap. Protocol based communication will ultimately replace current interfaces which will change many test paradigms.

DIFFICULT CHALLENGES

Table ITWG1 Summary of Key Test Drivers, Challenges, and Opportunities

Key Drivers (not in any particular order)	
Device trends	*Increasing device interface bandwidth (# of signals and data rates)*
	Increasing device integration (SoC, SiP, MCP, 3D packaging)
	Integration of emerging and non-digital CMOS technologies
	Complex package electrical and mechanical characteristics
	Device characteristics beyond one sided stimulus/response model
	3 Dimensional silicon - multi-die and Multi-layer
	Multiple I/O types and power supplies on same device
	Fault Tolerant Architectures and Protocols
Increasing test process complexity	*Device customization during the test process*
	Feedback data for tuning manufacturing
	Dynamic test flows via "Adaptive Test"
	Higher order dimensionality of test conditions
	Concurrent Test
	Maintaining Unit level Traceability
Continued economic scaling of test	*Physical and economic limits of test parallelism*
	Managing (logic) test data and feedback data volume
	Managing interface hardware and (test) socket costs
	Balancing Tool Capability, Multiple Insertions, System Test and BIST
Difficult Challenges (in order of priority)	
Cost of Test and Overall Equipment Efficiency	*Continues to be the primary driver for innovation. Traditional drivers for COT are started to be limited by OEE*
Test Development as a gate to volume production (Time to Market)	*Increasing device complexity driving more complex test development*
Detecting Systemic Defects	*Testing for local non-uniformities, not just hard defects*
	Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Screening for reliability	*Implementation challenges and effectiveness of burn-in, IDDQ, and Vstress*
	Erratic, non deterministic, and intermittent device behavior
	Mechanical damage during the testing process
	Multi-die stacks/TSV
	Power Management Issues
Future Opportunities (not in any order)	
Test program automation (not ATPG)	*Automation of generation of entire test programs for ATE*
Scan diagnosis in the presence of compression	*Collect better yield improvement and scan debug information*
Simulation and modeling	*Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process*
Convergence of test and system reliability solutions	*Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)*

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMS—micro-electromechanical systems

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

PIDS has four main sections: Logic, DRAM, Non-Volatile Memory, and Reliability. Relatively major changes from the 2010 Edition are listed under each section heading below:

LOGIC

- A new technology based on high-mobility alternate channel materials is introduced. It is anticipated that InGaAs will be used for *n*-channel and Ge for *p*-channel. The technology aims for similar speed performance as HP (high-performance) Logic but with lower power (lower V_{dd}). It is forecasted to be in production in 2018.
- There are minor changes for gate length and V_{dd} for smoothened curves (and trends) versus years.
- A metric to monitor dynamic power, CV^2, is added for all logic technologies.

DRAM

- Cell half-pitch is unchanged for near years, and slightly relaxed beyond 2020.
- For the storage cell capacitor, the dielectric equivalent oxide thickness (EOT) is relaxed beyond 2018.
- Introduction of $4F^2$ cell in 2013 is unchanged.

NON-VOLATILE MEMORY (NVM)

- There are changes in table format: (1) Charge-storage types of NVM, floating-gate and charge-trapping FETs, are separated from non-charge-based, two-terminal cells into different tables. (2) 3-D flash cells are grouped and have their own parameter values which might be different from those of 2-D cells.
- Poly half-pitch scaling is accelerated by 1 year.
- Transition from floating-gate flash to charge-trapping cell is delayed by 2 years to 2014.
- Transition from 3 bit/cell to 4 bit/cell is delayed by 2 years to 2021.
- Introduction of 3-D NAND is delayed by 1 year to 2016.

RELIABILITY

- A new category is introduced for highly reliable system (e.g., medical) with more stringent early failure rate that gets more stringent with time.
- The specification for long-term reliability is set at 1 FIT per chip. The more relaxed specification for up to 1000 FITs per chip for very small system is removed.
- The SRAM soft error rate is specified with FITs/chip rather than FITs/Mb.

DIFFICULT CHALLENGES

Table ITWG2 *Process Integration Difficult Challenges*	
Near-Term 2011-2018	***Summary of Issues***
1. Scaling Si CMOS	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain in new structures
2. Implementation of high-mobility CMOS channel materials	Basic issues same as Si devices listed above High-κ gate dielectrics and interface states (D_{it}) control CMOS (*n*- and *p*-channel) solution with monolithic material integration Epitaxy of lattice-mismatched materials on Si substrate Process complexity and compatibility with significant thermal budget limitations
3. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectrics Low leakage in access transistor and storage capacitor; implementing buried gate type/saddle fin type FET Low resistance for bit- and word-lines to ensure desired speed Improve bit density and lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
4. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Multi-level at < 20 nm nodes and 4-bit/cell MLC Non-scalability of tunnel dielectric and interpoly dielectric in flash memory – difficulty of maintaining high gate coupling ratio for floating-gate flash Few electron storage and word line breakdown voltage limitations Cost of multi-patterning lithography Implement 3-D NAND flash cost effectively Solve memory latency gap in systems
5. Reliability due to material, process, and structural changes, and novel applications.	TDDB, NBTI, PBTI, HCI, RTN in scaled and non-planar devices Electromigration and stress voiding in scaled interconnects Increasing statistical variation of intrinsic failure mechanisms in scaled and non-planar devices 3-D interconnect reliability challenges

Table ITWG2	*Process Integration Difficult Challenges*
	Reduced reliability margins drive need for improved understanding of reliability at circuit level Reliability of embedded electronics in extreme or critical environments (medical, automotive, grid...)
Long-Term 2019-2026	***Summary of Issues***
1. Implementation of advanced multi-gate structures	Fabrication of advanced non-planar multi-gate MOSFETs to below 10 nm gate length Control of short-channel effects Source/drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Identification and implementation of new memory structures	Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions Cost effective installation of high density 3-D NAND (512 Gb – 4 Tb) Implementing non-charge-storage type of NVM cost effectively Low-cost, high-density, low-power, fast-latency memory for large systems
3. Reliability of novel devices, structures, and materials.	Understand and control the failure mechanisms associated with new materials and structures for both transistor and interconnect Shift to system level reliability perspective with unreliable devices Muon-induced soft error rate
4. Power scaling	V_{dd} scaling Controlling subthreshold current or/and subthreshold slope Margin issues for low V_{dd}
5. Integration for functional diversification	Integration of multiple functions onto Si CMOS platform 3-D integration

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES

Radio frequency and analog/mixed-signal (RF and A/MS) technologies are critical technologies for rapidly diversifying semiconductor markets that include numerous applications for wireless and wireline markets. The roadmap contains the requisite technology elements for circuits used in wireless, wire-line, and, new for this year, low-frequency analog applications such as power management and display drivers. Products containing these circuits to meet market demands of increased functionality at lower cost per function are becoming key drivers for volume manufacturing and increased consumption of semiconductors.

SCOPE

The 2011 ITRS RF and AMS roadmap presents the challenges, technology requirements, and potential solutions for the basic technology elements (transistors and passive devices) used in RF and AMS circuits. The five technology-based devices are CMOS, silicon bipolar and BiCMOS, III-V compound semiconductor (bipolar and FET), passive on-chip, and high-voltage MOS (HVMOS) devices. The application frequency bands from 0 GHz to 0.4 GHz, 0.4 GHz to 30 GHz, and 30 GHz to 300 GHz generally drive different technology requirements.

CMOS—The CMOS roadmap reflects more accurately the RF and analog performance of the transistors in high-performance and low standby-power circuits. Other changes include: a more rigorous prediction of the effects of parasitic resistances and capacitances and the observations that the unity current gain cut-off frequency f_T increases faster than in given rgw 2009 roadmap and that f_{MAX} is lower in near-term due to parasitic effects.

SILICON BIPOLAR AND BICMOS—The key driving forces include speed, power consumption, noise and breakdown voltages. The changes are: 1) the NPN power-amplifier and general analog NPN parameters such as 1/f noise and current matching are not in the 2011 roadmap and 2) the high-speed 2011 roadmap aligns with ongoing trends and now includes applications associated with the expanded RF and AMS scope.

III-V COMPOUND SEMICONDUCTORS [BIPOLAR AND FIELD EFFECT TRANSISTORS (FET)]—Devices based on III-V compound semiconductors will continue to serve niche markets driven more by performance than cost and where silicon technology cannot meet the performance requirements such as high dynamic range or low noise. The RF and AMS roadmaps for GaAs PHEMT(2015), GaAs MHEMT(2019), InP HEMT(2021), GaN HEMT(2021) and InP HBT(2023) may end by the dates shown due to scaling limitations.

PASSIVE ON-CHIP DEVICES—The 2011 roadmaps addresses the challenges and requirements of on-chip passive devices, treats distributed passive devices that based on transmission lines for frequencies above 30 GHz, and contains discussions on "parasitics aware design" and improved definitions of all related figures of merit (FOMs).

HIGH-VOLTAGE MOS—The roadmap treats for the first time both HVNMOS and HVPMOS that are key for power-management and display-driver applications. The major FOMs for HVMOS are breakdown voltage, on-resistance, and the CMOS node with which the HVMOS devices are integrated. Due to the uncertainty in needing CMOS densities beyond the 90 nm generation, the 2011 HVMOS roadmap ends at the 90 nm node.

TRENDS—The following trends influence future roadmaps. Continued progress in shrinking dimensions and higher-frequency performance will be driven by market applications. Volume markets will be very cost sensitive and SiGe and RF CMOS will be utilized where their performance is adequate. The latter may further delay moving III-V R&D advances into production. The measurement of device parameters and FOMs at frequencies in the mm-wave bands will be key to understanding the physical mechanisms that limit device performance and to simulating accurately this performance. Establishing standardized methodologies for de-embedding devices parameters from the parasitics, especially above 50 GHz, will be essential for continued progress. International standards and their associated measurement methods are key enablers for success at all stages of RF and AMS innovation. Mesh-networks that use mobile millimeter-wave communications are very promising solutions for addressing the spectrum crunch. Because of this, much exploratory work on mobile devices at millimeter wavelengths exists. Within the domain now called "More than Moore," the following three emerging technologies are future candidates for RF transceiver functions of transistors, mixers, local oscillators, and resonators: graphene RF transistors, nanometer-sized spin-torque oscillators, and nano-resonators for tunable RF filters with high-quality factors made from nano-electro-mechanical-systems (NEMS) devices.

DIFFICULT CHALLENGES

Table ITWG3 RF and Analog Mixed-Signal (RF and AMS) Technologies Difficult Challenges

RF and Analog Mixed-Signal (RF and AMS) Technologies Difficult Challenges	Summary of Issues
CMOS	Many of the materials-oriented and structural changes being invoked in the digital roadmap degrade or alter RF and analog device behavior. Complex tradeoffs in optimization for RF and AMS performance occur as different mechanisms emerge as limiting factors, e.g., gate resistance, that greatly affect parasitic impedances in local interconnects. Fundamental changes of device structures, e.g., multiple-gates and silicon on insulator, to sustain continued digital performance and density improvements greatly alter RF and AMS characteristics. Such differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries.
Silicon Bipolar and BiCMOS	The primary challenge for the HS-NPN is increasing the unity current gain cut-off frequency f_T by more aggressive vertical profiles while still maintaining $f_{MAX} > f_T$, i.e. low base resistance and low base-collector capacitance (C_{BC}). The main challenge for the HS-PNP is increasing f_T by more aggressive vertical profiles. In addition to the inherent minority carrier mobility differences between electrons and holes, shrinking the vertical profile of a SiGe PNP is more challenging because it requires controlling the valence band offsets to avoid the appearance of parasitic barriers. Another challenge for the HS-PNP is the difficulty of the co-integration with HS-NPN and CMOS. This integration always adds more constraints on the HS-PNP fabrication.
III-V Compound Semiconductors [bipolar and field effect transistors (FET)]	The unique challenges are yield (manufacturability), substrate size, thermal management, integration density, dielectric loading, and reliability under high fields. Challenges common with Si based circuits include improving efficiency and linearity/dynamic range, particularly for power amplifiers. A major challenge is increasing the functionality of power amplifiers in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity requirements at the same or lower cost.
On-Chip Passive Devices	The co-integration of active and passive devices introduces process complexity and can lead to manufacturing control and costs challenges. The decreasing overall stack as well as the individual metal heights results in increasing resistive losses and vertical parasitic capacitances and limits the quality-factors of the on-chip integrated inductors, transformers, and capacitors.
High-Voltage MOS	Several aspects of high voltage devices and the associated base technology make it difficult and unlikely that the HV roadmap for the future will follow the lithographic shrink seen for CMOS because the HV designs can not take advantage of the lithography capability to shrink the intrinsic HV device dimensions, analog devices are usually large to improve the noise and mismatch, and the digital content of a HV chip is usually a small fraction of the chip area.

MICROELECTROMECHANICAL SYSTEMS (MEMS)

Micro-Electro-Mechanical Systems (MEMS) are fabricated using techniques similar to those used for integrated circuits (ICs) to create micrometer-sized mechanical structures (suspended bridges, cantilevers, membranes, fluid channels, etc.) that are often integrated with analog and digital circuitry. MEMS can act as sensors, receiving information from their environment, or as actuators, responding to a decision from a control system to change the environment. This first iteration of the ITRS MEMS focused on near-term (5 year) advances in device performance metrics, design and simulation, assembly and packaging, and testing.. A major conclusion reached is that while the back-end of MEMS manufacturing (packaging and testing) consumes two thirds of the total manufacturing cost, and continues to rise, virtually all R&D investment has been on the front-end of manufacturing (devices and process development). The development of a consensus opinion that documents possible solutions for the issues facing the industry, which is the primary output from our technology roadmapping, can be used as a tool to optimize R&D investment that meets the critical manufacturing needs to address the issues faced in the back-end of MEMS manufacturing.

SCOPE

The ITRS MEMS technology roadmap focuses on the key technologies associated with mobile internet devices, such as smart phone and tablet computers. The key MEMS device technologies considered are: accelerometers and gyroscopes, microphones, and RF MEMS, including resonators, varactors, and switches. These applications represent the fastest growing segment in MEMS manufacturing, according to 2011 market forecasts by iSuppli, Yole Development, and SEMI. The roadmap considered both the evolution of discrete MEMS devices and integrated MEMS technologies. It also reviews emerging MEMS applications, including optical filters, picoprojectors, the electronic nose, microspeakers, and ultrasound devices.

DISCRETE MEMS ACCELEROMETERS, GYROSCOPES, AND MICROPHONES

Discrete MEMS accelerometers and gyroscopes are expected to see continuous incremental improvement in resolution, bias, and drift, with resolutions improving by a factor of 2, from 1000 μg to 500 μg for accelerometers and 100μ °/s/√Hz to 50μ °/s/√Hz for gyroscopes, by 2017. MEMS microphones are expected to see an improvement in sensitivity from -42 dB (V/Pa) to -38 dB (V/Pa) at 1 kHz. The greatest challenge faced by manufacturers of discrete MEMS devices comes from the required cost and size reductions. The cost of MEMS accelerometers and gyroscopes is predicted to decrease from $0.60 to $0.20 and $2.70 to $1.20 per die by 2017, respectively, with no known solutions at the present time.

RF MEMS

RF MEMS resonators, varactors, and switches are also expected to see a continuous incremental improvement in performance. The greatest challenge that these devices face in order to penetrate into the mobile internet market is increasing their reliability from the present typical mean times to failure. Meeting this challenge requires advancing knowledge of the physics of failure in materials used in MEMS, reliability simulation tools, and better methods for accelerated lifetime testing. RF MEMS also specifically call out requirements for inductors with quality factors $Q > 50$ integrated at the package level and methods for minimizing package interconnect length and loading.

INTEGRATED MEMS

The greatest challenges by manufacturers of integrated MEMS for mobile internet device technologies were in relation to their integration path towards the Inertial Measurement Unit (IMU); a device that incorporates a 3-axis accelerometer, 3-axis gyroscope, 3-axis magnetometer (compass), and a pressure sensor (altimeter). The greatest cause for concern for multimode sensor technologies relates to testing. The cost of testing has been continuously increasing yet the price of the devices continues to fall; a trend that cannot be sustained. The challenges of testing are further compounded by the increasing complexity of the tests, which require testing the multiple functionalities (acceleration, angular rate, direction, and elevation) of the IMU.

DIFFICULT CHALLENGES

Table ITWG4 MEMS Difficult Challenges

Challenge	Need
Assembly and Packaging	• Standardization for MEMS packaging to support integration. • Packages are needed that reduce or eliminate mechanical stress and enhance hermeticity. • Package data that can be used to accurately predict the effect of the package on device performance.
Device Testing	• Move from testing at the device level towards more testing towards the wafer level. • Validated tools to predict device performance from wafer tests. • Methodologies to "Design for Test."
Reliability	• More knowledge of the physics of failure is required to develop accelerated life tests. • Need to share information. Individual solutions exist but are not being generalized across the industry.

EMERGING RESEARCH DEVICES

The 2011 Emerging Research Devices (ERD) chapter provides an ITRS perspective on emerging research memory, logic, and information processing device technologies and serves as a bridge between CMOS and the realm of nanoelectronics beyond the end of ultimately scaled CMOS. It further addresses memory and information processing nanoarchitectures related to and made possible by emerging research devices.

Two technology-defining domains are addressed: 1) extending the functionality of the CMOS platform via continued scaling and heterogeneous integration of new technologies, and 2) stimulating invention of a new information processing paradigm. The relationship between these domains is schematically illustrated in Fig. 1. The expansion of the CMOS platform by conventional dimensional and functional scaling is often called "More Moore". The CMOS platform can be further extended by the "More-than-Moore" domain. This is a new subject included in this chapter in which added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". On the other hand, new information processing devices and architectures, often referred to as "Beyond CMOS" technologies, have been and remain the main subjects of this chapter. The heterogeneous integration of "Beyond CMOS", as well as "More-than-Moore", into "More Moore" will extend the CMOS platform functionality to form ultimate "Extended CMOS".

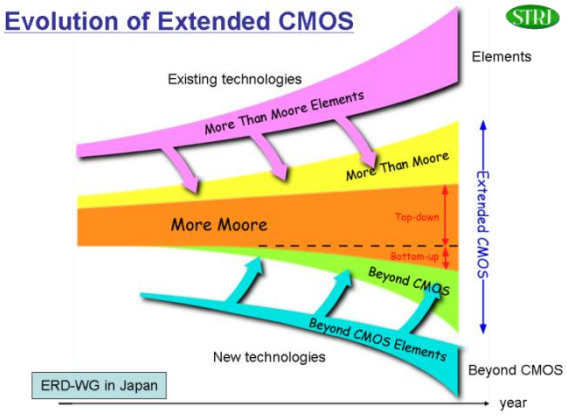


Figure ITWG1 Relationship among More Moore, More-than-Moore, and Beyond CMOS

In particular the ERD chapter surveys, assesses and catalogs viable new memory and information processing devices and systems architectures for their long-range potential, technological maturity, and identifies the scientific/technological challenges gating their acceptance by the semiconductor industry as having acceptable risk for further development. This 2011 ERD chapter includes the new More-than-Moore section to address long term alternative technology entries, currently for wireless devices and, in the future, for power devices, image sensors, etc. Also included is an expansion of the Memory Device section to include two new subsections: one on Storage Class Memory (to include Solid State Drive Memory) and another on the "Select Device" required for a crossbar memory applications.

In addition emerging research memory and logic device Technology Entries in the ERD chapter are constantly scrutinized to evaluate their technological maturity and potential performance. These criteria are used to determine their readiness either to transition as potential solutions to the PIDS (Process Integration, Devices, and Structures) and the FEP (Front End Processing) chapters or to be removed from further consideration in the ERD chapter. Two such technologies were transitioned to PIDS and FEP in 2010-2011. One is the Spin Transfer Torque Magnetostatic RAM (STT-MRAM) in the memory section and the other is n-channel InGaAs and p-channel Ge channel and source/drain replacement materials in Si MOSFET structures.

An expanded "benchmarking" section assesses the potential of each emerging research device technology entry considered in this chapter to perform its intended memory or information processing function benchmarked against current memory or CMOS technologies, all at their full maturity. The results of this evaluation are that several emerging memory technologies (e.g. STT-MRAM, ReDOX ReRAM, Phase Change Memory, etc.) have potential to succeed flash

beyond the 16nm generation. Conversely, more work is required on the logic or information processing devices before potential candidates to supplement CMOS can be identified.

DIFFICULT CHALLENGES

Table ITWG5 Emerging Research Devices Difficult Challenges

Difficult Challenges – 2018– 2026	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile, and non-volatile memory technologies to replace SRAM and / or FLASH for manufacture by 2018.	SRAM and FLASH scaling in 2D will reach definite limits within the next several years (see PIDS Difficult Challenges). These limits are driving the need for new memory technologies to replace SRAM and possibly FLASH memories by 2018. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond 2018 - 2026	Develop 2nd generation new materials to replace silicon (or InGaAs, Ge) as an alternate channel and source/drain to increase the saturation velocity and to further reduce Vdd and power dissipation in MOSFETs while minimizing leakage currents for technology scaled to 2018 and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in this development.
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and reduce to practice a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A new information processing technology must also be compatible with a systems architecture that can fully utilize the new device. A new non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for a new systems architecture. Bridge the gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials Reliability issues should be identified & addressed early in the technology development
Invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless/analog and eventually in power devices, MEMS, image sensors, etc.	The industry is now faced with the increasing importance of a new trend, "More than Moore" (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security and entertainment.

EMERGING RESEARCH MATERIALS

WHAT'S NEW

The 2011 Emerging Research Materials (ERM) chapter is an updated version of the 2009 ITRS ERM. The 2011 ERM Chapter device materials section has been reorganized to better align with the ERD organization. The 2011 ERM reviews materials for ERD Memory and Logic applications, lithography including novel resist, front end process and process integration and devices applications, interconnects, and assembly and package applications. The ERM chapter also identifies metrology, modeling, and environmental safety and health research needed to support these materials for their potential applications. In 2011, the ERM has added a transition table to note materials that are being added to the scope or are being removed from the chapter. While these ERMs have properties that make them attractive as potential solutions to future technology needs, significant progress is required for them to be adopted in future technologies.

ERM for Emerging Research Devices includes materials for Memory and Logic, which includes alternate channel materials for extending CMOS and Beyond CMOS devices. In 2011, materials for n-III-V and p-Ge alternate channel material devices have been transitioned to the PIDS and FEP chapters due to their maturity, but p-III-V and n-Ge are being retained by the ERM. A critical assessment of alternate channel materials was completed and the results did not change significantly from 2009. Lithography Materials continues to include resist materials and directed self-assembly materials for extending lithography. A critical assessment of DSA was completed and indicates that progress in reducing defect densities has raised interest in this technology to potentially extend scaling. Materials and Processes for Front End Processes progress has been made on deterministic dopant placement and there is interest in molecular layer doping to potentially replace implant doping. Interconnect materials has transitioned Ru and Zr ultra-thin barrier layers to the Interconnect Chapter, but retained self-assembled organic barrier layers. Interconnects also includes low κ ILD materials to extend Cu interconnects, multiwalled carbon nanotubes, graphene, and single crystal nanowires interconnect replacements. Assembly and Package Materials reviews nanometals for low temperature solders and anisotropically conducting interconnect materials, carbon nanotubes for high current chip to package interconnects, and the use of nanoparticles and macromolecules to deliver package polymers to meet the multiple conflicting properties required for application to underfill, mold compound, and multiple adhesive applications.

DIFFICULT CHALLENGES

The current set of ERM Difficult Research Challenges is summarized in Table ITWG6. Perhaps ERM's most difficult challenge continues to be delivering material options, with controlled desired properties in integrated structures, in time to impact insertion decisions. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the sub 20 nanometer scale and be extensible to nanometer scale. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community.

Directed self-assembly for lithography must also demonstrate the ability to pattern features in high density with low defect density. This requires defect detection tools and methodologies that can identify isolated defects in large areas. Furthermore, simulation and modeling tools are needed that can identify materials properties that need to be controlled to support defect densities, and assess the impact of process variability on defect density.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled orientations. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties.

Table ITWG6 Emerging Research Materials Difficult Challenges

Difficult Challenges – 2018– 2026	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile, and non-volatile memory technologies to replace SRAM and / or FLASH for manufacture by 2018.	SRAM and FLASH scaling in 2D will reach definite limits within the next several years (see PIDS Difficult Challenges). These limits are driving the need for new memory technologies to replace SRAM and possibly FLASH memories by 2018. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond 2018 - 2026	Develop 2nd generation new materials to replace silicon (or InGaAs, Ge) as an alternate channel and source/drain to increase the saturation velocity and to further reduce Vdd and power dissipation in MOSFETs while minimizing leakage currents for technology scaled to 2018 and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in this development.
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and reduce to practice a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A new information processing technology must also be compatible with a systems architecture that can fully utilize the new device. A new non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for a new systems architecture. Bridge the gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials Reliability issues should be identified & addressed early in the technology development
Invent and reduce to practice long term alternative solutions to technologies that address existing MtM ITRS topical entries currently in wireless/analog and eventually in power devices, MEMS, image sensors, etc.	The industry is now faced with the increasing importance of a new trend, “More than Moore” (MtM), where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law“. Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security and entertainment.

FRONT END PROCESSES

The Front End Processes (FEP) Roadmap focuses on future process requirements and potential solutions related to scaled field effect transistors (MOSFETs), DRAM storage capacitors, and non-volatile memory (Flash, Phase-change, and ferroelectric). The purpose of the FEP chapter is to define comprehensive future requirements and potential solutions for the key front end wafer fabrication process technologies and the materials associated with these devices. This encompasses the tools, and materials, as well as the unit and integrated processes starting with the wafer substrate and extending through the contact silicidation processes and the deposition of strain layers. The following specific technology areas are covered: *logic devices, including high performance, low operating power, and low stand-by power; memory devices, including DRAM, flash, phase-change, and FeRAM; starting materials; surface preparation; thermal/thin films/doping*; *plasma etch; and CMP*.

Recent MOSFET scaling performance has been compromised primarily due to unacceptable leakage/power delivered by sheer geometric scaling. To stay on the performance at low power curve, new materials have now been put into production for transistor gate stack fabrication. Non-planar multi-gate devices have been announced as new approaches to device structure, and within the next several years we expect to see the introduction of additional approaches, as well as new materials to increase channel mobility. The challenges associated with integration of these diverse new materials and structures are the central theme of the FEP chapter.

Continued transistor performance at low power scaling is expected to require the replacement of traditional planar CMOS devices with non-classical devices which include fully depleted non-planar devices and possibly planar versions. The transition from extended bulk CMOS to non-classical device structures is not expected to take place at the same time for all applications and all chip manufacturers. Instead, a scenario is envisioned where a greater diversity of technologies are competitively used at the same point in time—some manufacturers choosing to make the transition to non-classical devices earlier, while others emphasize extensions of bulk technology. This is reflected in the High-Performance and Low-Power Device Technology Requirements Tables FEP2, FEP3 and FEP4 in the FEP Chapter, by the projection of requirements for multiple approaches in the transition years from 2013 through 2019.

In the logic section, high-κ gate dielectrics with metal gate electrodes are shown to be used in production but continued scaling of equivalent oxide thickness (EOT) below 0.7 nm while preserving electrical performance and reliability is shown as a challenge. Channel strain engineering to increase mobility has become an integral part of MOSFET transistor scaling now and is expected to continue in the near future. Continued improvement in strain engineering effectiveness and application to new device structures is identified as an FEP difficult challenge.

It is expected that high mobility channels based on III-V (In-Ga-As) and Ge will replace Si channels for nFETs and pFETs respectively around 2018. The selective incorporation of these high mobility channels on Si in a VLSI scheme is a clear challenge.

Additional challenges include continued scaling and abruptness of shallow junctions and the control of parasitic and contact resistances. Variability in the placement of dopant atoms and their final location, along with variations resulting from process control introduced by patterning, cleaning and deposition constitute dominant scaling challenges. These require considerable effort in developing new variability tolerant process techniques. The introduction of new materials is also expected to necessitate new techniques to dope and electrically activate silicon. Series resistance is critical in the near term and needs to be addressed to achieve the goals through 2015. The limited thermal stability of most high-κ mobility materials is expected to place new constraints on thermal budgets associated with dopant activation.

In the memory area, stand-alone DRAM device manufacturing has narrowed to the stacked capacitor approach. Therefore, the Technology Requirements table and text for DRAM trench capacitor has been removed and the DRAM section is implicitly aimed at stacked capacitor technologies. The DRAM tables were still in review and not changed for 2011, but will be addressed and updated in 2012. It is expected that high-κ materials will be required for the floating gate Flash memory interpoly dielectric by 2012 and for tunnel dielectric by 2013.

In starting materials, it is expected that bulk silicon will continue to dominate but alternative silicon-on-insulator (SOI) substrates will find continued usage, particularly for special product applications. Substrate interaction with new channel materials will become an increasingly important consideration. Also, an important difficult challenge is the need for the next diameter generation 450 mm silicon substrate, although 300 mm parallel approaches are also shown.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as higher-κ dielectrics, metal gate electrodes, and mobility-enhanced channel materials. Cleaning processes are expected to become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed.

In etch, wafer gate CD variation solutions are now available from advanced process control (APC). At the 28nm technology node and beyond, the presence of line width roughness (LWR) is becoming the biggest portion of CD variation The LWR is at best staying constant as the line width shrinks, which makes it a major scaling concern. Current methods of quantification need to be standardized to allow the industry to address the problem. With high-κ dielectrics and metal gates in production, etch processes with sufficient selectivity and damage control for use with these materials have been identified. As non-planar transistors become necessary, dry etch becomes much more challenging. FinFET configurations bring new constraints to selectivity, anisotropy, and damage control.

Chemical-Mechanical Planarization (CMP) is becoming more important for Front End Processing. Being a critical step in the formation of shallow trench isolation for many nodes, its need and uniformity control has become even more important in flash memory devices and in the implementation of gate-last metal gate integration schemes. Uniformity, selectivity, and pattern density dependency continue to be challenges for CMP processes and significant improvements were made to the CMP tables to reflect these new requirements.

DIFFICULT CHALLENGES

Table ITWG7 Front End Processes Difficult Challenges

Difficult Challenges ≥ 11 nm	*Summary of Issues*
	Strain Engineering - continued improvement for increasing device performance - application to FDSOI and Multi-gate technologies
	Achieving low parasitics (resistance and capacitance) and continued scaling of gate pitch
	Achieving DRAM cell capacitance with dimensional scaling - finding robust dielectric with dielectric constant of ~60 - finding electrod material with high work function
	Achieving clean surfaces free of killer defects - with no pattern damage - with low material loss (<0.1 A)
	450mm wafers - meeting production level quality and quantity
Difficult Challenges < 11 nm	*Summary of Issues*
	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
	Introduction of high mobility channels (based on III-V and Ge) to replace strained Si
	Lowering required DRAM capacitance by 4F2 cell scheme or like, while continuing to address materials challenges
	Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
	Continued EOT scaling below 0.7 nm with appropriate metal gates
	Continued charge rention with dimensional scaling and introduction of new non-charged based NVM technologies

LITHOGRAPHY

Extending optical lithography beyond 2011 has become increasingly difficult. Single optical exposure has reached its limit at the 40 nm half-pitch (hp). 32 nm hp Flash devices are being manufactured today using 193 nm double patterning (DP) as a way of extending the half-pitch while keeping the numerical aperture (NA) and wavelength constant. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm hp and Flash starts to test the limits at the 22 nm hp in 2013. It is at this point that non-optical lithography must be introduced into manufacturing to ensure a smooth transition beyond 22 nm. Extreme ultraviolet lithography (EUVL) has been gaining significant momentum with several manufacturers taking delivery of pilot line tools. Some have even announced plans to purchase production tools that will be delivered as early as 2012. If EUVL should not be ready on time, the industry will likely extend DP to multiple patterning (MP). Other non-optical lithography may also be used in a complementary fashion for small volume applications and/or prototyping.

LONG-TERM DIFFICULT CHALLENGES

The long-term challenges depend on the solutions chosen from the potential solution table. The transition to new technologies might even be necessary at larger half-pitches. All solutions will require new infrastructure support, which means solutions must be narrowed to two or three options at an early stage. This will allow financial support to be focused on developing the technology and its infrastructure.

As EUVL remains the leading candidate for the 22 nm and 16 nm half-pitches, extending it to higher resolutions becomes a significant long-term challenge. From what we know today, designs of 0.5NA or larger at the current wavelength will necessitate either an eight-mirror unobscured or six-mirror center obscuration design. The eight-mirror design will have more diminished reflectance because of the added mirrors, requiring higher power sources for an equivalent wafer throughput. The angular spread in the six-mirror design is narrower, thus demanding a smaller field size and perhaps longer track length. The increase in NA will pose significant challenges in the depth of focus for both designs. Furthermore, to overcome shadowing and other 3D effects on the mask, absorber materials, absorber thickness, and multilayer stacks will have to be optimized.

An alternative solution path would be to reduce the EUVL wavelength to 6.x nm. In the near term, this path would inherit all the current challenges of EUVL, from source availability to mask infrastructure and resist performance. Multiple patterning with EUVL will also be an option, bringing with it added process difficulties and cost of ownership.

Current resist difficulties such as line width roughness, sensitivities, and resolution will become even greater. Additionally, requirements in overlay, defect, and CD control will be more stringent.

Many technological challenges will need to be overcome for maskless lithography (ML2) to be feasible for cost-effective semiconductor manufacturing. It will probably require die-to-database inspection of wafers to replace die-to-database inspection of masks. If imprint lithography finds its way as a volume manufacturing solution, mask fabrication, defectivity control, and metrology will become even more challenging as imprint lithography templates have the same dimensions as the wafer pattern.

Direct Self Assembly (DSA) is a new star on the horizon with the promise to overcome the potential limitations of the other next-generation lithographies. The molecular structure of the imaging material drives the sub-lithographic feature sizes and control. The major challenge is the requirement for defect-free processing. Whether this is a chemical engineering or a fundamental physical issue is still unclear.

In addition to these many challenges is the need for better supporting infrastructure, including metrology tool availability to measure and control key parameters such as critical dimension uniformity (CDU), overlay, material thicknesses, and defects.

DIFFICULT CHALLENGES

Table ITWG8 Lithography Difficult Challenges

Near Term Challenges (2011-2018) *(16nm Logic/DRAM @ HVM; Flash 11nm @ optical narrowing with 16nm in HVM)*
Multiple patterning - cost, throughput, complexity
Optical mask - complexity with SRAF, long write time, cost
EUV source power to meet throughput requirement; Defect "free" EUV masks availability; mask infrastructure availability; EUV mask in fab handling, storage, and requalification.
Resist at 16nm and below that can meet sensitivity, resolution, LER requirements
Process control on key parameters such as overlay, CD control, LWR at 16nm HVM
Retooling requirements for 450mm transition (Economic & Technology Challenges)
Long Term Challenges (2019 - 2025) *(11nm @HVM)*
Higher source power, increase in NA, chief ray angle change on EUV; Mask material and thickness optimization
Defect free DSA processing
Infrastructure for 6.Xnm Lithography or multiple patterning for EUVL 13.5nm
Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect
Early narrow and implement ~2 options with viable infrastructures support

HVM—high volume manufacturing

INTERCONNECT

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of a CMOS integrated circuit, along with providing necessary power and ground connections. The process scope begins at the contact level with the pre-metal dielectric and continues up to the wire bond pads, describing deposition, etch and planarization steps, along with any necessary etches, strips and cleans. A section on reliability and performance includes specifications for electromigration and calculations of delay. The fundamental development requirement for interconnect is to meet the high-bandwidth low-power signaling needs without introducing performance bottlenecks as scaling continues. Although the Interconnect Technical Working Group (TWG) continues to forecast the use of copper as the primary conductor in a dual-damascene architecture through the end of the 15-year forecast horizon, much of the current research and development focuses on new challenges and trends associated with 3D integration, new materials, processes, and emerging technology.

For 2011, Interconnect performance is at the forefront as a key challenge to achieve overall chip performance. Air gap structures are now considered a mainstream potential solution for the ILD, recognizing their increased maturity. The ITRS team firmly believes that any substantial reduction in effective κ will not be achieved by further materials improvements of porous ultra-low-κ ($\kappa \leq 2$) but by the use of air gap structures. For low-κ, this is the end of materials solutions and the beginning of architecture solutions. Delays in the emergence of quality ALD processes prevent the deposition of the required sub-2 nm barriers, and are a top concern. Discussions on 3D interconnects have been moved out of the emerging interconnect section, with TSVs nearing production. In addition, the ITRS chapter contains significant new content on the search for Cu replacements and the need to consider interconnect requirements for the inevitable replacement for the FET switch. There are more radical options beyond even carbon nanotubes − including molecular interconnects, quantum waves and spin coupling − that are in the infant stages of development but, in each case, the goal is propagating terabits/second at femtojoules/bit.

INTERCONNECT SUMMARY 2011

- 3D and air gaps moved out of emerging sections
- Low-κ – unchanged for second time in 10 years due to lack of progress in materials
  - Air gaps coordinated with design expected to be solution for κ bulk < 2.0
  - Accelerated in 2011 with κ bulk < 2.4
- Jmax current limits are width dependent − a new concern
- Barriers (<2.0 nm) and nucleation layers are a critical challenge
  - ALD integration is still being investigated, including the combination with appropriate lower k dielectrics and barrier metals
  - Approaches of new liners (Co, Ru and others) stacked with barrier layers are proliferating
  - Capping metal for reliability improvement
- New interconnect 3D TSV Roadmap tables
- Cu contact need expected > 2013
- Multiple emerging interconnect solutions are being researched
- First-principle consideration for native interconnects
  - To distinguish interconnect from switching properties of emerging devices and materials – CNT, graphene, nanowires, etc.

DIFFICULT CHALLENGES

Table ITWG9 Interconnect Difficult Challenges

Five Most Critical Challenges ≥ 16 nm	*Summary of Issues*
Material *Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	*The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.*
Manufacturable Integration *Engineering manufacturable interconnect structures, processes and new materials*	*Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool*
Reliability *Achieving necessary reliability*	*New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.*
Metrology *Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.*
Cost & Yield for Manufacturability *Manufacturability and defect management that meet overall cost/performance requirements*	*As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.*

Five Most Critical Challenges < 16 nm	*Summary of Issues*
Material *Mitigate impact of size effects in interconnect structures*	*Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.*
Metrology *Three-dimensional control of interconnect features (with it's associated metrology) is required*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.*
Process *Patterning, cleaning, and filling at nano dimensions*	*As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.*
Complexity in Integration *Integration of new processes and structures, including interconnects for emerging devices*	*Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.*
Practical Approach for 3D *Identify solutions which address 3D structures and other packaging issues*	*3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.*

CMP—chemical mechanical planarization DRAM—dynamic random access memory

FACTORY INTEGRATION

Factory Integration (FI) is one of the key sections of the International Technology Roadmap for Semiconductor (ITRS) that strives to integrate all the factory components in order to efficiently produce the required products in the right volumes on schedule while meeting cost targets. In order to keep up with the Moore's law, it is paramount to sustain the decades-long trend of 30% per year reduction in cost per function that requires capturing all possible factory cost reduction opportunities.

FACTORY INTEGRATION FOCUS AREAS 2011/12

In addition to working on the five factory integration sub-sections and cross-ITWG challenges, the FI ITWG also evaluated key technology focus areas that impact the factory integration near-term and long-term needs and also cuts across all the FI thrusts in 2011/12.

WASTE REDUCTION AND PROACTIVE VISUALIZATION

As the cost of manufacturing increases, it is becoming imperative to focus on other areas of cost reduction in parallel with Si scaling. The FI ITWG discussed a cost driving concept and the relevant metrics in the preceding 5 years and concluded that waste reduction is a critical concept to drive manufacturing to meet the Moore's Law cost trend.

Waste is the most common sense of productivity loss and can be a metric that will drive comprehensive effort in each ITWG to attain high productivity and cost reduction.

The ITRS needs to discuss, firstly, on the target setting for waste reduction deduced from Moore's Law or equivalent derivatives, secondly, how each ITWG can incorporate this new theme into their activities, and, finally, how TR Tables can express their requirements along with the waste reduction. This discussion should include comprehensiveness of the metrics needed for the roadmap. Apparently energy and resource waste reduction is becoming another axis in addition to the Si scaling.

One of the most effective waste reduction areas is production equipment's Dandori operations (the operations which are peripheral and preparatory to the main thread of production operations). Dandori operations can be classified into three logical areas; (1) those residing in the production equipment, (2) those residing in the interface between the production equipment and factory, and, (3) those residing in factory operation. The first area is to be dealt with by the equipment supplier and device maker collaboratively. "In-situ chamber cleaning" and "chamber seasoning" are well known example affiliated to this logical area. Carrier and/or lot exchange is a known waste in the 2nd area. The frequent change of process recipes due to small lot operation is known to cause considerable waste in tool operation and it is affiliated to the third logical area.

More study is needed to prepare for the general waste reduction approaches. Such approach should include systematic measurement and visualization methods of wastes. The systematic knowledge on waste is used as guidance to the effectiveness and reliability of equipment design and operation practices in addition to the conventional CIP effort.

Such approaches are effective for WTW (Waite Time Waste) and EOW (Equipment Output Waste) visualization and reduction. WTW for a wafer can be measured by simply summing up all the wait time for that wafer. Such measured data is not necessarily used for the improvement planning. There are numerous interactions between wait times and the other factors such as resource availability and other wafers' waiting for the production tools. To visualize the causes of waits calls for more study on the principal interactions. EOW can be characterized relatively simply for a single piece of equipment. The factory level EOW can be measured likewise, but EOW proactive visualization for EOW improvement planning is significantly difficult due to the interactions between tools and localized Work in Progress (WIP) status. Factory simulator needs to be hooked up with the visualization tool for the planning and evaluation after improvement implementation. Industry needs to work on the standardization of triggers for state transitions of factory resources and products. Especially production equipment should provide reasonable granularity to facilitate waste reduction in the equipment.

FUTURE MANUFACTURING REQUIREMENTS AND 450 MM TRANSITION CHALLENGES

In keeping up with the Moore's law, the semiconductor industry looks at increasing the wafer size as one viable option in addition to device innovations for 30% improvement in cost/cm^2 (primary goal) and 50% cycle time reduction. The last wafer size transition from 200 mm to 300 mm occurred 10 years ago and it is showing clear indication of ~30% cost improvement. As 300 mm wafer production enters its 4th major technology generation (45 nm), the industry will work on

transitioning to 450 mm, in a seamless manner from the current 300 mm technology. The Next Generation Fab activity is expected to address the seamless improvement usable both to 300 mm significant improvement and 450 mm. Discussions on the 450 mm wafer transition within the FI ITWG and also with the other ITWG uncovered several technical as well as business challenges. More factory services specific to 450 mm are expected to be systematically studied and captured in the roadmap in 2010 and after.

ENERGY CONSERVATION

The primary goal of energy conservation is to reduce facility operation cost by enabling facility demand based utilization model in which energy conservation plays a pivotal role. The Factory Integration team worked on several initiatives within the facilities and production equipment sub-team to define energy conservation related challenges and the outcome of this work is reflected as a metric (tool idle versus processing energy consumption) in the Facilities technology requirements table. Equipment sleep mode means that the equipment support units such as pumps will be shut down when no wafers are processed (i.e., when the tool is idle). The FI ITWG needs to work on energy conservation more intensively from 2012 and beyond based on the waste reduction and proactive visualization schemes.

MIGRATION FROM REACTIVE TO PREDICTIVE OPERATIONS

All of the previous focus areas will benefit significantly from a movement of factory operations from a reactive mode to a predictive mode. Reactive practices such as fault detection, preventive and unscheduled maintenance, and real-time scheduling and dispatch have been used and optimized in the past to achieve quality and productivity objectives. Unfortunately these techniques cannot ultimately eliminate waste (product, downtime, cycle time, etc.) because they wait for the problem to occur before addressing it, or, as in the practice of preventive maintenance, employ conservative and potentially wasteful practices in order to avoid an unexpected event. With the move to predictive, systems will be modeled and problems will be predicted before they occur. This means that (1) fault detection should migrate to fault prediction, eliminating scrap on fault occurrence, (2) predictive maintenance can reduce unscheduled downs and allow for relaxing of conservative (and wasteful) maintenance practices, (3) predictive scheduling shall minimize wait time and cycle time waste, (4) virtual metrology shall provide metrology values for all wafers, and (5) yield prediction should be used to control processes and systems to quality and productivity targets directly. A key challenge in the migration from reactive to predictive is the ability to establish accurate, robust, reconfigurable, real-time updateable and understandable models that are the basis for prediction. A key focus for prediction will be techniques for improving prediction accuracy and for utilizing prediction accuracy information (along with the prediction itself) to optimize prediction systems.

SUMMARY

The Factory Integration chapter of the ITRS focuses on integrating all the factory components needed to efficiently produce the required products in the right volumes on schedule while meeting cost targets. The Factory Integration chapter provides the technical requirements by the five sub-groups and also the proposed potential solutions. It also provides Factory Integration related challenges from the crosscut issues and key focus areas that need to be addressed in order to keep up with the technology generation changes, productivity improvements and at the same time maintaining decades-long trend of 30% per year reduction in cost per function.

For more information and details on Technology Requirements and Potential Solutions, access the electronic chapter links for Factory Integration highlighted as links throughout this chapter and online at *http://www.itrs.net*.

DIFFICULT CHALLENGES

Table ITWG10	*Factory Integration Difficult Challenges*
Difficult Challenges through 2019	*Summary Of Issues*
1. Responding to rapidly changing, complex business requirements	• Increased expectations by customers for faster delivery of new and volume products (design → prototype and pilot → volume production) • Rapid and frequent factory plan changes driven by changing business needs • Ability to load the fab within manageable range under changeable market demand, e.g., predicting planning and scheduling in real-time • Enhancement in customer visibility for quality assurance of high reliability products; tie-in of supply chain and customer to FICS operations
2. Managing ever increasing factory complexity	• Quickly and effectively integrating rapid changes in process technologies • Increased requirements for high mix factories. Examples are (1) significantly short life cycle time of products that calls frequent product changes, (2) the complex process control as frequent recipe creations and changes for process tools and frequent quality control criteria due to small lot sizes • Manufacturing knowledge and control information need to be shared as required among factory operation steps and disparate factories • Need to concurrently manage new and legacy FICS software and systems with increasingly high interdependencies • Ability to model factory performance to optimize output and improve cycle time for high mix factories • Need to manage clean room environment for more environment susceptible processes, materials, and, process and metrology tools • Addressing need to minimize energy resource usage and waste; e.g., need to integrate fab management and control with facilities management and control • Comprehending increased purity requirements for process and materials Providing a capability for more rapid adaptation, re-use and reconfiguration of the factory to support capabilities such as rapid new process introduction and ramp-up. This includes a challenge of supporting evolution of a FI communication infrastructure to support emerging capabilities beyond interface A. • Supporting adoption and migration of equipment communication protocol standards to meet ITRS challenges and be in sync with emerging technologies in systems communication and management such as XML and cloud computing. • Meeting equipment design challenges in maintaining yield and improving maintenance practices resulting from movement to new process materials that may be corrosive, caustic, environmentally impacting, molecularly incompatible etc. • Addressing factory integration challenges to assess and integrate EUV systems into the factory infrastructure • Addressing AMC challenges through possibly changing factory operation approach (e.g, maintaining vacuum in specific areas), as well as providing necessary interfaces, information and technologies (e.g., virtual metrology and APC).

Table ITWG10	*Factory Integration Difficult Challenges*
	• Maintaining equipment availability and productivity while managing increase in senors and systems within and outside the equipment, coordinated to support new paradigms (e.g., management of energy expended by the equipment and the fab in general, movement from reactive to fully predictive) • Linking yield and throughput prediction into factory operation optimization • Real-time simulation in lock-step with production for operations prediction
3. Achieving growth targets while margins are declining	• Ability to visualize cost and cycle time for systematic waste reduction from all aspects. • Reducing complexity and waste across the supply chain; reducing white space in cycle times • Minimize the cost of new product ramp up against the high cost of mask sets and product piloting
4. Meeting factory and equipment reliability, capability and productivity requirements per the Roadmap	• Increased impacts that single points of failure have on a highly integrated and complex factory • More equipment reliability, capability and productivity visualization that can be used bidirectionally between equipment suppliers and users for more efficient task sharing • Design-in of equipment capability visualization in production equipment; design-in of APC (R2R control, FD , FC and SPC) to meet quality requirements • Equipment supplier roadmap for equipment quality visualization and improvement, and, reduction of Equipment Output Waste. • Reduction of equipment driven NPW (non-product wafers) operations that compete for resources with production wafers and Dandori operations[1] • Meeting wait-time waste factory level management targets; developing wait-time waste reporting for tools; supporting standardized fab-wide equipment state information management. • Moving from reactive to predictive paradigm for scheduling, maintenance and yield management
5. Emerging factory paradigm and next wafer size change	• Addressing issues in movement from lot-based to single-wafer processing and control • Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness. 450mm era: Effecting architectual and other changes as necessary at an affordable cost to maintain or improve wafer-throughput-to-footprint levels in migration to 450mm
Difficult Challenges Beyond 2019	*Summary of Issues*
1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	• Ability to utilize task sharing opportunities to keep the manufacturing profitable such as manufacturing outsourcing • Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing business models • Scalability implications to meet large 450 mm factory needs • Cost and task sharing scheme on industry standardization activity for industry infrastructure development
2. Managing ever increasing factory complexity	• Higher resolution and more complications in process control due to smaller process windows and tighter process targets in many modules • Complexity of integrating next generation lithography equipment into the factory • More comprehensive traceability of individual wafers to identify problems to specific process areas • Comprehensive management that allows for automated sharing and re-usages of complex engineering knowledge and contents such as process recipes, APC algorithms, FD and C criteria, equipment engineering best known methods

Table ITWG10	*Factory Integration Difficult Challenges*
3. Increasing global restrictions on environmental issues	• Need to meet regulations in different geographical areas • Need to meet technology restrictions in some countries while still meeting business needs • Comprehending tighter ESH/Code requirements • Lead free and other chemical and materials restrictions • New material introduction
4. Post-conventional CMOS manufacturing uncertainty	• Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements on factory design • Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition • Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency

Notes for Table ITWG10

[1] Dandori operations: Peripheral equipment related operations that are in parallel or in-line and prior to or following to the main thread PE operations. So-called in-situ chamber cleaning is another good example than NPW operations.

ASSEMBLY AND PACKAGING

Moore's Law scaling has continued for transistor count and cost, but as we entered the deep submicron era, scaling for frequency and power efficiency has not kept up. This is due, in part, to the interconnect materials limitations, but it is primarily due to the lack of scaling advantages in packaging technologies. The developments in wafer-level packaging, system in package and the coming 3D revolution will enable scaling advantages in packaging. This scaling will support a continuation of the rapid pace of progress achieved by the electronics industry. New design tools, new package architectures, new material, new processes and new equipment will all be required to achieve that goal. The historical evolution in packaging is becoming a revolution to meet the changing demands of the consumer-dominated markets for electronic products. This revolution is supported by worldwide cooperation in Roadmaps to identify the difficult challenges and the emergence of consortia where cooperation in this effort reduces duplication of effort.

DIFFICULT CHALLENGES

The difficult challenges identified for the 2011 Assembly & Packaging Roadmap are presented in Table ITWG13. There has been a rapid pace of change in materials, processes and architectures to meet challenges greater than or equal to 16nm in the last few years and progress continues. The challenges for geometries below 16 nm reflect the fundamental changes associated with continued scaling. The challenges are complex and will require substantial innovation.

Table ITWG11 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥16 nm	*Summary of Issues*
Impact of BEOL including Cu/low- κ on packaging	Direct wire bond and bump to Cu for very fine pitch due to thin wire limits
	Dicing for ultra low-κ dielectric (includes k <2.5eff and air gaps)
	Improved fracture toughness of dielectrics
	Interfacial adhesion
	Mechanical reliability for chip-package interconnect (requires co-design due to chip-package interaction)
	Methodologies for measurement of critical properties needed
	Probe damage for copper/ultra low κ
Wafer-level packaging	I/O pitch for small die with high pin count
	Solder joint reliability for tight pitch/low stand-off interconnect
	Compact ESD structures
	CTE mismatch compensation for large die and fanout die
Coordinated design tools and simulators to address chip, package and substrate co-design	Mix signal co-design and simulation environment
	Rapid turn-around modeling and simulation
	Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis
	Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching)
	System level co-design is needed now
	EDA for "native" area array is required to meet the Roadmap projections
	Models for reliability prediction
Interposers and embedded components	CTE mismatch for large interposers
	Defect density at very thin interfaces
	Low-cost embedded passives: R, L, C
	Embedded active devices
	Quality levels required not attainable on chip
	Electrical and optical interface integration
	Wafer-level embedded components
Thinned die packaging	Handling technologies for thin wafers (particularly for bumped wafers)
	Impact of different carrier materials (organics, silicon, ceramics, glass, laminate core)
	Establish new process flows
	Reliability
	Testability

Table ITWG11	*Assembly and Packaging Difficult Challenges*
Difficult Challenges ≤ 16 nm	*Summary of Issues*
Close gap between chip and substrate, improved organic substrates	Increased wireability at low cost
	Improved impedance control and lower dielectric loss to support higher-frequency applications
	Improved planarity and low warpage at higher-process temperatures
	Low-moisture absorption
	Increased via density in substrate core
	Silicon I/O density increasing faster than the package substrate technology
High current density packages	Low-resistance contacts
	Electromigration
Flexible system packaging	Conformal low-cost organic substrates
	Small and thin die assembly
	Handling in low-cost operation
3D assembly and packaging	Thermal management
	Design and simulation tools
	Wafer-to-wafer bonding
	Through wafer via structure and via fill process
	Singulation of TSV wafers/die
	Test access for individual wafer/die
	Cost of TSV
	Bumpless interconnect architecture
Package cost does not follow the die cost reduction curve	Margin in packaging is inadequate to support investment required to reduce cost
	Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	Electromigration at high current density for interconnect (die, package)
	Thermal dissipation
	Improved current density capabilities
	Higher operating temperature
High-frequency die	Substrate wiring density to support >20 lines/mm
	Lower loss dielectrics
	"Hot spot" thermal management
	Package substrates with lines and spaces below 10 microns
System-level design capability to integrated chips, passives and substrates	Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability and cost of complex systems very difficult
	-Complex standards for information types and management of information quality along with a structure for moving this information will be required.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages)
	-Biological interfaces will require new interface types
Power integrity	- Power supply quality
	- Power delivery in stacked die
	-Reducing power supply voltage with high device switching currents

ENVIRONMENT, SAFETY, AND HEALTH

The 2011 ESH section of the overall Roadmap continues to reflect the fact that the principles of successful ESH program execution remain largely independent of the specific technology thrust advances to which they are applied. Thus, many ESH Roadmap elements, such as the Difficult Challenges and the Technology Requirements, bear strong similarities to those in the 2009 Roadmap. As a result, the four basic ESH Roadmap strategies continue as in the 2009 Roadmap, namely:

- To understand (characterize) processes and materials during the development phase
- To use materials that are less hazardous or whose byproducts are less hazardous
- To design products and systems (equipment and facilities) that consume less raw material and resources
- To make the factory safe for employees and the surrounding communities

By applying these strategies as essential elements to success, the industry continues to be an ESH as well as a technology leader. Semiconductor manufacturers have adopted a business approach to ESH which uses principles that are integrated with manufacturing technologies, products, and services.

A unique consideration in the ESH section of the Roadmap results from the fact that while the Roadmap is by intent and execution a technology-focused document, the ESH section must necessarily comprehend and address various policy and regulatory issues. Any failure to do so could jeopardize the implementation of successfully developed technologies. Such issues for ESH were explicitly recognized for the first time in the 2009 Roadmap by the introduction of ESH Categories and Domains, as will be reviewed shortly. The 2011 ESH Roadmap extends this concept by the introduction of two new Subcategories (requirements have data, or no data available) to reflect the availability of Roadmap quality goals and metrics to address the ESH goals presented.

The ESH roadmap identifies challenges when new wafer processing and assembly technologies move through research and development phases, and towards manufacturing insertion. Following the presentation of ESH Domains & Categories (including the new Subcategories) in Table ESH2, ESH technology requirements are listed in Tables ESH3–7. Potential technology and management solutions to meet these challenges are proposed in Figures ESH1–3. Successful resolution of these challenges will best be realized when ESH concerns are integral in the thinking and actions of process, equipment, and facilities engineers; as well as those of chemical/material and tool suppliers; and finally those of academic and consortia researchers. ESH improvements must also contribute to (or at minimum, not conflict with) enhanced cost, technical performance, and product timing. They must inherently minimize risk, public and employee health & safety effects, and environmental impact. Successful global ESH initiatives must be timely, yet far reaching, to ensure long-term success over the Roadmap's life.

For 2011 two critical areas, both focused on materials, will be where efforts are concentrated. The first is defining research needs that decrease polarization of public/government policy expectations versus future technology needs, where critical materials are needed or new materials required to assure future technology. The second area is determining how to specify technology requirements in non-quantifiable or non-data supported terms where data do not exist, are not representative, or do not have granularity for defining a technical objective—while the objective remains important for ESH.

To better address these key challenges of defining research needs, determining technology requirements and mitigating future regulatory and compliance restrictions, we have added a new strategic element in this year's Roadmap, to build on our existing industry business processes. We have committed to integrating 'Green Chemistry' Principles into the Roadmap, to serve as both a framework and process for the industry, in addressing the full range of ESH challenges. By adoption of this Green Chemistry approach at the outset of the technology life cycle, starting at the chemical design phase, this will enable the industry to maximize the time for addressing future ESH challenges. For the ESH TWG, the focus will be on proactive engagement with stakeholder partners and customers to reset strategic focus of the roadmap.

DIFFICULT CHALLENGES

Table ITWG12	*Environment, Safety, and Health Difficult Challenges*
Difficult Challenges ≥ 16 nm	*Summary of Issues*
Overall challenge	There is a need for Roadmap quality goals and metrics need to be defined for a substantial number of ESH technology requirements
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials achieve timely insertion in manufacturing, while protecting human health, safety, and the environment. Given the global options for R&D, pre-manufacturing, and full commercialization, these methodologies must recognize regional regulatory/policy differences, and the overall trends towards lower exposure limits and increased monitoring. • *Chemical Data Availability*: Comprehensive ESH data for many new, proprietary chemicals/materials is incomplete, hampering industry response to the increasing regulatory/policy requirements on their use. In addition, methods for anticipating and forecasting such future regulatory requirements are not well developed.. • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and how process by-products are formed. Also, while methods used to obtain such information are becoming more standardized, their availability varies depending on the specific issue being addressed.
Process and equipment management	• *Process Chemical Optimization* There is a need to develop processes and equipment meeting technology requirements, while at the same time reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). • *Environment Management:* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations (including the capability for component isolation in waste streams) for such hazardous and non-hazardous emissions and by-products can be properly addressed. Global Warming Emissions Reduction: There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Water and Energy Conservation:* There is a need for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization:* There is a need for more efficient chemical/material utilization, with improved reuse/recycling/reclaiming of them and their process emissions and by-products. • *Byproducts Management*: There is a need for improved metrology for by-product speciation. • *Chemical Exposure Management:* There is a need to design-out chemical exposure potentials and the requirements for personal protective equipment (PPE) • *Design for Maintenance:* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life:* There is a need to develop effective management systems to address issues related to equipment end-of-life reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities consumption and for more efficient thermal management of cleanrooms and facilities systems. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to reduce total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics:* There is a need for methodologies to define and measure a technology generation's sustainability. • *Design for ESH:* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products. • *End-of-Life Reuse/Recycle/Reclaim:* There is a need to design facilities, equipment and products to facilitate these end-of-life issues
Difficult Challenges < 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials achieve timely insertion in manufacturing, while protecting human health, safety, and the environment. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use
Process and equipment management	· *Chemical Reduction*: There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Environment Management:* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations for such hazardous and non-hazardous emissions and by-products can be addressed. • *Water and Energy Conservation:* There is a need to reduce water and energy consumption, and for innovative energy- and water-efficient processes and equipment.

Table ITWG12	*Environment, Safety, and Health Difficult Challenges*
	• *Consumables Optimization:* There is a need for more efficient chemical/material utilization, including their increased reuse/recycle/reclaim (and of their process emissions and by-products). • *Chemical Exposure Management:* There is a need to design-out chemical exposure potentials and personal protective equipment (PPE) requirements. • *Design for Maintenance:* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life:* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient thermal management of cleanrooms and facilities systems. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics:* There is a need for methodologies to define and measure sustainability by technology generation, as well as at the factory infrastructure level. • *Design for ESH:* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products, with methodologies to holistically evaluate and quantify the ESH impacts of facilities operations, processes, chemicals/materials, consumables, and process equipment for the total manufacturing flow. • *End-of-Life Reuse/Recycle/Reclaim*: There is a need to design facilities, equipment and products to facilitate these end-of-life issues

YIELD ENHANCEMENT

The 2012 edition of the Yield Enhancement Chapter has major changes compared to previous years and a reorientation of the scope of the chapter. The Yield Enhancement Chapter was revised deleting no longer updated subchapters. Therefore, the Yield Enhancement chapter consists now of two subchapters, 'Wafer Environment and Contamination Control' (WECC) and 'Characterization, Inspection and Analysis' (CIA), the latter one building upon the basis of the previous 'Defect Detection and Characterization' chapter.

WECC continues providing contamination control limits for media as UPW, chemicals, pure gases and air in clean rooms and clean compartments. Control limits have been updated based on their known yield impact in critical process steps. Specific attention has been paid to the impact of AMC (Airborne Molecular Contamination) in enclosed wafer environments as FOUPs. The assessment and description of solutions improving the contamination situation in FOUPs has been initialized. It is a segment of ongoing consultation with experts from Factory Integration (FI). Means of production as reticles are considered an important topic for WECC. They are consequently included in the compilations now and in the future. Process specific and compartment specific contamination limits have been detailed. Reviewing reliable and fast quantification methods for these contaminants is scheduled task and will render results during the period 2012/2013. To evaluate the effects of contamination on new manufacturing technologies as EUV lithography and to recommend limit values is within the scope of work for 2012 review.

The scope of CIA was defined in 2011 facing the demands in broad applications as e.g. 'More Moore' and 'More than Moore' technologies. Also power electronics, mechatronics and MEMS applications, furthermore, characterization, inspection and analysis demands and requirements from packaging and assembly have been taken into account. This major change of the scope was decided in the meetings of 2010/2011. Tables and potential solutions will be prepared for the revision in 2013.

Currently, the most important key challenge is estimated to be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high through put. Furthermore, it is a dare to identify yield relevant defects under a vast amount of nuisance and false defects. As a challenge with second priority process stability vs. absolute contamination level was identified. This includes the correlation to yield test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness. In 2011 with the change of the scope of the subchapter to 'Characterization, Inspection and Analysis', a new key challenge with lower priority was identified and added: Detection of organic contamination on surfaces – The detection and speciation of non-volatile organics on surfaces is currently not possible at the manufacturing site. There is no laboratory scale instrumentation available.

In 2011 'next generation inspection' was identified as the first key challenge in the long term. As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This pathfinding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.

Furthermore, in the long term the key challenges in - line defect characterization and analysis and next generation lithography were identified:

The specific revisions to the subchapters were:

- Wafer Environment and Contamination Control (WECC)

  The WECC sub chapter was placed at the beginning of the yield chapter taking into account the attention of the community to this activity.

  The table YE3 was structured to a side-by-side comparisons of contamination control limits for the clean room environment and for the interior of FOUPs (direct wafer environment). Limit values for YE3 have been checked carefully, reviewed and missing values been added.

FOUP cross-contamination problems from wafer and material outgassing together with the prevention and assessment of this challenge has been addressed in a so call integrated approach. The effects of measures determining and controlling FOUP contamination, their effects per process step and q-time have been evaluated together with Factory Integration.

Potential solutions have been tabulated for the FOUP cross-contamination challenge as well as for monitoring challenges for AMC in the clean room environment.

- Characterization, Inspection & Analysis (CIA)

  The scope of the subchapter was extended as discussed above. The tables YE 4, 5 and 6 were revised based upon the technology specific critical dimensions.

DIFFICULT CHALLENGES

Table ITWG13 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Detection and identification of Small Yield Limiting Defects from Nuisance - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
Non-Visual Defects and Process Variations – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.	Systematic Mechanisms Limited Yield (SMLY), resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
Process Stability vs. Absolute Contamination Level – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
Detection of organic contamiantion on surfaces – The detection and speciation of non volatile organics on surfaces is currently not possible in the fab. There is no laboratory scale instrumentation available.	A possible work around is the use of NEXAF at a synchrotron radiation facility.

Table ITWG13	*Yield Enhancement Difficult Challenges*
Difficult Challenges < 16 nm	*Summary of Issues*
Next Generation Inspection - As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node.	Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.
In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	Data volume + quality: strong increase of data volume due to miniaturization The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Next generation lithography - Manufacturing faces several choices of lithography technologies in the long term, which all pose different challenges with regard to yield enhancement, defect and contamination control.	

METROLOGY

Metrology requirements continue to be driven by advanced lithography processes, new materials, and Beyond CMOS materials, structures, and devices. The push for EUV Lithography is driving the development of new metrology equipment for masks. Existing Critical Dimension metrology is approaching its limits and requires significant advances to keep pace with the needs of patterning. Another key challenge to critical dimension metrology is tool matching. Near term precision (measurement uncertainty) requirements for the next few years can be met using single tools. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continue to drive metrology to provide measurements for new channel materials including III-V film stacks, higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. 3D device structures such as FinFETs place significantly more difficult requirements on dimensional and doping metrology. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation. Potential solutions for bonded wafer overlay are now available. For Beyond CMOS R&D, many areas of graphene metrology have advanced but putting them into volume manufacturing will require challenging R&D. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, metrology R&D is working with other Beyond CMOS materials.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 16 nm ½ pitch Metrology needs after 2019 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG16 presents the ten major challenges for metrology.

Table ITWG14 Metrology Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Directed Self Assembly Lithography, complicated 3D structures such as FinFET & MuGFET transistors, capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Although there have been significant advances in off-line characterization of FinFET structures, the recent announcement that a FinFET transistor will be used in manufacturing at the 16 nm 1/2 pitch has placed renewed emphasis on the near term need for in-line metrology for dimensional, compositional, and doping measurements. The materials properties of block co-polymers result in new challenges for lithogrpahy metrology. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 16 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-16 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

MODELING AND SIMULATION

Modeling and Simulation is the virtual counterpart of semiconductor device and chip fabrication and characterization: Computer programs are used to predict the geometries, chemical composition (dopants, defects, etc.) and mechanical stress of devices, their electrical performance and reliability, and finally the behavior of circuits and systems. The overall aim of Modeling and Simulation is to support the development of real-world technologies, devices, circuit and systems by providing information which is more difficult, more costly, less efficient or too time-consuming to obtain from experiments, and in this way to reduce development times and costs. To enable this, Modeling and Simulation tools must contain appropriate physical models including appropriate parameter settings, and also meet various requirements in terms of generality of application, speed of simulation, complexity of the applications which can be addressed, and, last but not least, user interfaces and interactions. In turn, dedicated research and development activities on Modeling and Simulation capabilities are needed.

In order to best meet the needs of the users of simulation tools in industry and research, the Modeling and Simulation group in the ITRS has also in 2011 based its work strongly on the industrial requirements, both from own assessments and from the results of the other groups in the ITRS, which deal with the various areas of process technology, integration, and fabrications issues. Starting from thorough review of all their texts and presentations and detailed discussions with these groups, again so-called crosscut sections have been prepared for the Modeling and Simulation chapter. The main part of the Modeling and Simulation chapter was prepared based on these crosscuts and an overall assessment of the state-of-the-art. In the following, the main elements of the chapter are summarized especially in view of the changes made compared with the 2009/2010 ITRS.

Similar to earlier years, the Modeling and Simulation Difficult Challenges are emphazised in the beginning of the chapter. The titles of all ten challenges have been kept unchanged from 2010. The six short-term challenges refer in 2011 to nodes until 14 nm including. Because of the developments of the industrial needs and the state-of-the-art, the detailed contents of nearly all of these challenges were significantly changed, as displayed in Table MS1 of the 2011 Modeling and Simulation Chapter. One example is that multiple patterning, although currently the favorite technological option, is no more mentioned as a simulation challenge, due to the progress obtained in the development of models and tools. An example for the impact of changes of preferred technological options to the Modeling and Simulation challenges is the update of the channel materials to be considered in the simulation of diffusion and (de)activation, and in nanoscale device simulation. The long-term challenges now refer to nodes smaller than 14 nm. Here, only the contents of the first three of them were slightly modified.

Similar to these crosscuts with the other groups of the ITRS, there are also strong links between the areas covered by the Modeling and Simulation chapter, ranging from the area of equipment simulation through processes, devices, interconnects and circuits up to packages. Also in 2011 the Modeling and Simulation chapter contains seven subchapters which deal with the various levels of modeling: *Equipment / Feature Scale modeling*, *Lithography Modeling*, *Front-end Process Modeling*, *Device Modeling*, *Interconnects and Integrated Passives Modeling*, *Circuit Modeling*, and *Package Simulation*. Furthermore, there are four topics which crosscut these seven areas, namely *Materials Modeling*, *Reliability Modeling*, *Modeling for Design Robustness, Manufacturing and Yield*, and *Numerical Methods and Interoperability of Tools*. Whereas the scopes of these subchapters have not changed compared to 2009, the requirements described therein have considerably evolved based on the development of the industry and the state-of-the-art in modeling and simulation. This also holds for the Modeling and Simulation requirements displayed in tables MS2a and MS2b, and the accuracy specifications given in table MS3. Major trends captured in these texts include the development of technological options in lithography which request in the *Lithography Modeling* subchapter among others Source Mask Optimization and close coupling between deposition, lithography and etching simulation, and the transfer of some device architectures and channel materials from the ERD and ERM chapters to the PIDS and FEP sections of the roadmap, which lead to important adaptations especially of the *Front-End Process Modeling* and of the *Device Modeling subchapter.* Another important trend is the further increasing demand for co-simulation in various respects, including electro, thermal and mechanical effects, length scales from transistors through chips and packages to fabrication equipment, and covering not only performance but also its variability, reliability and reliability under variability. This trend has materialized in various subchapters, especially those on *Device Modeling*, *Interconnects and Integrated Passives Modeling*, *Circuits Element Modeling*, *Materials Modeling*, *Reliability Modeling*, and of course *Modeling for Design Robustness, Manufacturing and Yield*.

The requirement for new modeling capabilities and for co-simulation, and the further growing importance of new device architectures and new materials further increase the need for interdisciplinary activities and long-term research. A vigorous research effort at universities and research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry. The shortage of research funds continues to be even more severe than the technical challenges summarized above. For example, several Modeling and Simulation requirements listed in preceding issues of the ITRS had in this 2011 issue to be delayed in time because sufficient R&D could not be done due to insufficient research funding.

DIFFICULT CHALLENGES

Table ITWG15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	*Summary of Issues*
Lithography simulation including EUV	Complementary lithography
	Simulation of defect inspection and characterization, influences/defect printing. Mask optimization including defect repair or compensation
	Simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including EMF and resist effects, and extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
	Predictive and separable resist models (e.g., mesoscale models) including line-edge roughness, accurate profiles, topcoat and substrate (underlayer) interactions, etch resistance, adhesion, mechanical stability, leaching, swelling or slimming, and time-dependent effects in in single and multiple exposure
	Resist model parameter calibration methodology (including kinetic transport and stochastic parameters)
	Fast, predictive simulation of ebeam mask making (single-beam and multibeam) including short and long range proximity corrections
	Simulation of directed self-assembly of sublithography patterns
	Modeling lifetime effects of equipment and masks, including lens and mirror heating effects
	Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
	Modeling metrology equipment and data extraction for enhancing model calibration accuracy
	Modeling of pellicle effects and pellicle defects simulation (incl. double patterning, self-aligned patterning)
Front-end process modeling for nanometer structures	Coupled diffusion/(de)activation/damage/stress models and parameters including low-temperature, SPER, millisecond and microwave processes in Si-based substrate, that is, Si, SiGe, Ge-on-Si, III/V-on-Si (esp. InGaAs-on-Ge-on-Si), SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers. Accurate models for Stress-Induced Defects
	Implantation models for ions needed for new materials
	Models for alternative implantation methods: Plasma doping (e.g. for FinFETs), cluster implantation, cyro or hot implants (incl. self-annealing)
	Diffusion in advanced gate stacks
	Predictive segregation and dose loss models
	Modeling of interface and dopant passivation by hydrogen or halogens
	Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping, diffusion, activation
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Efficient and robust 3D meshing for moving boundaries

Table ITWG15	*Modeling and Simulation Difficult Challenges*
	Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability bahavior during operation
Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction
	Linked equipment/feature scale models (including high-κ metal gate integration, flows for RIE processes, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills, evolution during transformation and densification
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Pattern/microloading effects in radiative annealing or plasma processing
	Propagation of process variations into circuit block simulation
	Simulation of wafer polishing, grinding and thinning
	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations
	Modeling of impact of consumables (e.g. resists, slurries, gas quality ….) on process results
Nanoscale device simulation capability: Methods, models and algorithms	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
	Efficient models and tools for analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (incl. material models) to investigate new memory devices like redox resistive memories, PCM/PRAM, etc.
	Models for gate stacks with ultra-thin/high-k dielectrics for all channel materials addressed above w.r.t. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport
	Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure , dopant and material variations in order to assess the impact of variations on statistics of device performance
	Physical models for novel channel materials, e.g., p-type Ge and compound III/V (esp. n-type InGaAs-on-Ge-on-Si) channels … : Band structure, defects/traps, ...
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation. Coupling between atomistic process and continuum or atomistic device simulation
	Reliability modeling for ultimate CMOS and new memory devices
	Commercial device simulators (software) for STT and redox resistive memories
	Physical models for (mechanical) stress induced device performance for advanced architectures (esp. FinFET) and/or novel materials
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension

Table ITWG15	*Modeling and Simulation Difficult Challenges*
	Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers
	Signal integrity modeling for 3D ICs
	Identify effects and apply/extend models which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects)
	Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces
	Dynamic simulation of mechanical problems of flexible substrates and packages
	Models for electron transport in ultra fine patterned interconnects
	Simulation tools for die, package and board that allow for coherent co-design
Circuit element and system modeling for high frequency (up to 300 GHz) applications [1]	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains - including manufacturability
	Introduction of new model features including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling
	Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
	Scalable active component models for circuit simulation of new multigate MOSFET like double gate FDSOI, FinFET …
	Scalable passive component models [2] for compact circuit simulation, including interconnect, transmission lines, …
	Scalable circuit models [2] for More-than-Moore devices including switches, filters, accelerometers, …
	Compact models for new memory devices, such as PCM, and standardisation of models for III/V (esp. InGaAs-on-Ge-on-SI) devices
	Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations
Difficult Challenges < 14 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Layer stacks for gates, junctions and and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, transport properties, reliability, breakdown, and leakage currents including band structure, phonon coupling, tunneling from process/materials and structure conditions 2) Models for novel integrations in 3D interconnects including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications 4) Accumulation of databases for semi-empirical computation

Table ITWG15	*Modeling and Simulation Difficult Challenges*
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping and doping by chemical functionalization, quantum dots, atomic electronics, multiferroic materials and structures, materials for non-charge-based Beyond-CMOS devices)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry (esp. edge effects / edge roughness), interfaces and bias on transport for carbon-based nanoelectronics (carbon nanotubes and monollayer/bilayer graphene structures)
	Compact models for maturing emerging devices
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, fast and efficient optical interconnect models of larger domains
	Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects)
	Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

Notes for table:

[1] 3 times frequency of envisioned applications (100 Ghz) because of harmonics/linearity

[2] In More than Moore, scalability refers to the ability to model litho-defined device variations

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables includes increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables undergo several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2010. The ORTC Glossary has not been updated in 2010, but definition proposals will be considered for the 2012 Update, which kicked off at the Incheon ITRS meetings in Korea in December, 2011.

OVERVIEW OF 2011 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds thousands of units per month of ICs from a manufacturing site using "production tooling." Furthermore, a second company must begin production within three months (see Figure 2). To satisfy this timing definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

It was mentioned in the Introduction section of the ITRS Executive Summary, but it is worth repeating, that there continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets.

During the 2003 ITRS development, an attempt was made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology "node" manufacturing in 2003. Since the contacted metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM stagger-contacted M1 half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that some of the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance). Some companies also referenced the timing for doubling of functionality on a given product (for example the doubling of logic gates or memory bits) as a measure of "node" advancement. This approach of measuring technology progress complicates the "node" relationship, because density improvements can be accomplished by design improvements added along with linear lithographic feature size reduction.

Additional confusion has developed due to the technology "node" references in Flash memory product announcements, and Flash technology received increased emphasis in both the 2005 and 2007 ITRS. For example, Flash product cell density is defined by the un-contacted poly-silicon (poly) interconnect half-pitch, rather than a metal 1 (M1) half-pitch (the key feature which drives density in DRAM and MPU and ASIC products). Also, very aggressive Flash memory Cell Area Factor (see Glossary) improvements have been added by Flash cell designers in order to aggressively reduce costs and meet the rapidly ramping demand for non-volatile memory (NVM) storage. Additional complications for Flash technology tracking result from the option to provide "equivalent scaling" through three-dimensional (3D) layers of Flash cells, as a trade-off with reduced half-pitch technology. The 3D Flash technology is anticipated to be in production beginning 2016, and receives special modeling considerations in the PIDS chapter and also the 2011 ORTC Table 2a,b and Table 5.

The International Roadmap Committee (IRC) decided in the 2007 ITRS roadmap that the best way to minimize confusion between the ITRS and individual company public announcements was to continue the separate tracking of the various

technology trend drivers by product—DRAM, MPU/ASIC, and Flash. As mentioned earlier, the MPU/ASIC and DRAM product half-pitches are now both defined by a common reference to the M1 stagger-contact, while the Flash NVM product is referenced to un-contacted poly dense parallel lines (refer to Figure 1). Individual TWG tables will utilize the product table header line items that are most representative of the technology trend drivers for each table.

Due to the emphasis on separate product trend tracking, no common product technology header is required. Only the year of production of the referenced technology line item is required as the minimum ITWG table header. In each of the roadmaps since the 2007 ITRS, the technology trends and the functional (transistors, bits, logic gates) or characteristic (speed, power) performance associated with the individual product groups (DRAM, Flash, MPU, ASIC) are emphasized. Individual company references that wish to compare to the ITRS must now reference the specific product technology trend line item, as further defined by the ITRS Executive Summary and Glossary.

Individual product technology trends continue to be monitored, and the most recent TWG survey update is indicating that the DRAM historical trend has tracked close to the average 2.5-year cycle (*cycle = one-half reduction per two cycle periods) trend through 2008. However the 2010 PIDS DRAM survey indicated a 1-year pull-in of the M1 Half Pitch timing, beginning 2009/45 nm, and continuing on a 3-year technology cycle to 2026/6.3nm.,. The modeled and calculated projection trends may produce slight differences from the actual survey results, however the timing which influences the Grand Challenges and Potential Research and Development solutions are consistent with the average trends of latest survey results.

In the most recent Flash technology survey, the overall lithography resolution continues to be driven at the most leading edge by the feature size trend from Flash product. For example, as is described in additional detail below, the uncontacted polysilicon half-pitch of FLASH memories is now projected to be even further ahead of DRAM stagger-contacted M1 half-pitch (by four years by 2011). A two-year lead by the Flash uncontacted polysilicon half-pitch is considered equivalent (in lithographic processing difficulty) to a one-year lead of the DRAM stagger-contacted M1 half-pitch, and this additional timing lead increase is therefore causing Flash memory technology to continue to drive leading-edge lithography. Please see the Glossary section for additional detail on the "Year of Production" timing definition.

The 2011 ITRS table technology trend targets continue as annualized targets from 2011 through the 15-year Roadmap horizon in 2026. However, per previously established IRC guidelines, the 2011 ITRS retains the *definition of a technology trend cycle time as the period of time to achieve a significant advancement in the process technology. To be explicit, a technology trend cycle time advancement continues to be defined as the period of time to achieve an approximate 0.71× reduction per cycle (precisely 0.50× per two cycles). Refer to Figures ORTC1 and ORTC2.

Please note from the 2011 ITRS Table ORTC-1 that the timing of a technology cycle remains different for a particular product. For example, the DRAM stagger-contact half-pitch M1 in the 2011 ITRS wason an average 0.71× reduction every two and one-half years (0.50×/5-years) timing cycle until 2008/59 nm). After 2008, as mentioned above, the DRAM M1 trend is forecast to pull-in one year and then continue on a three-year cycle through the 2026/6.3 nm target. The annual multiplier for the three-year cycle timing is 0.8909× reduction per year, which is used to calculate the interim annual trend targets (examples: 2011/36 nm, 2020/10 nm).

After taking into account the available industry PIDS survey data and other ITWG and IRC inputs, consensus was reached on a new Flash product technology timing model (based on the uncontacted polysilicon half-pitch definition). The Flash uncontacted polysilicon half-pitch is now pulled in to 2010/24nm] and then set on a four-year cycle timing pace to 2020/10 nm. At the 2020 point, the Flash trend is equal to the original 2009 and 2010 version target and returns to a 3-year pace to 2022/8nm; and then remain flat to 2026/8nm due to anticipated Flash cell design limitations. The Lithography ITWG also continues to use the Flash uncontacted polysilicon half-pitch (now projected to be numerically four years "ahead" of the DRAM stagger-contacted M1 half-pitch in 2010) to drive the technology process equipment being used to achieve that target. After 2010/24nm trend model target, the Flash uncontacted polysilicon half-pitch is expected to turn to a fouryear timing cycle, ahead of, but at a slower pace (4-year cycle) than the DRAM trend (3-year cycle).In response to Design TWG data and model inputs, the 2011 ITRS, the MPU (and high-performance ASIC) (MPU/hpASIC) Product Trend cycle timing (based on the same stagger-contact M1 half-pitch definition as DRAM) remains unchanged to the 2009 and 2010 ITRS versions. After analysis of historical data and consensus agreement by the ITWGs and IRC, the MPU M1 half-pitch continues to be delayed behind the new 1-year-accelerated DRAM trend; however the MPU/hpASIC is set on a two-year cycle (reducing in half every 4-years) timing pace through 2013/27 nm. Therefore, at the 2012/32 nm point, the MPU/hpASIC M1 target crosses over the DRAM M1 cycle timing target. From the 2013/27 nm point, the MPU/hpASIC M1 contacted half-pitch will turn to a three-year timing cycle through the end of the roadmap in 2026, and remain very slightly ahead of the DRAM Trend.

The MPU/hpASIC final physical gate-length (phGL) was significantly revised in the 2008 Update, and then again during the 2009 ITRS work. The targets for a portion of the historical trend remain unchanged from the 2003 ITRS, in which the timing was set at a two-year cycle (0.5×/4-years; 0.8409×/year) from 1999 through the 2003/45 nm point. From that point through the 2009/29 nm target, the trend was adapted to track actual data points provided by the FEP and PIDS ITWGs. From the 2009/29 nm point the model tracks the PIDS survey data, and utilizes trend targets calculated by using a 3.8-year timing (reducing in half every 7.6 years; or 0.9128 reduction per year) cycle through the end of the Roadmap to 2026/5.9 nm. The Lithography and FEP ITWGs revised their agreement on a new consensus variable ratio between the printed gate length targets and the final physical gate length, which includes etch.[4]

The low-operating-power ASIC gate length targets are likewise adapted to the new PIDS survey data (by shifting their introduction timing relative to the MPU printed and physical gate lengths); and a new standby-power physical gate length line item was added in the 2008 Update and is updated in the 2011 ORTC tables by extending the trend out to 2026. To match new work by the PIDS, a Printed Low Operating Gate Length trend was added, and also a variable ratio between printed and final physical low-operating power gate length. For the 2012 Update, work will be done with PIDS and FEP and Design TWGs to determine if only two trends, high-performance and low power are needed, instead of the three types.

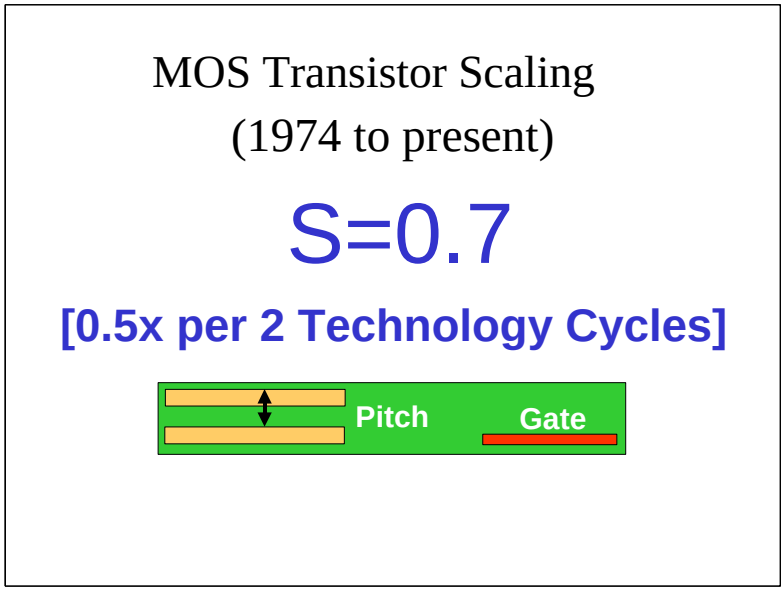


Figure ORTC1 *MOS Transistor Scaling—1974 to present*

[4] *Special thanks to John Boyd, Principle Process Analyst at UBM Techinsights and Dick James, Senior Technology Analyst at Chipworks for data contributions to Front End Processes' ITRS modeling for physical gate length.*

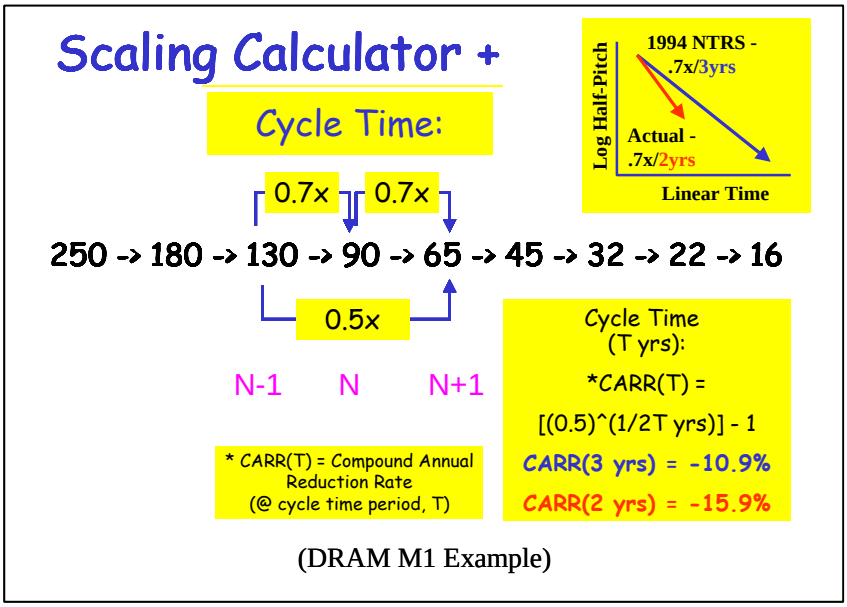


Figure ORTC2 *Scaling Calculator*

ROADMAP TIMELINE

The 2011 edition of the Roadmap maintains a 15-year projection, from 2011 as a reference year and through 2026. The timing trends of the future technology pace of the DRAM product, in past roadmaps, has represented the leading edge for stagger-contacted M1 half-pitch, and is forecast to return to the three-year cycle (three years between 0.71× reduction of the feature size) after 45 nm/2010, unchanged from the 2008 edition. In the 2008 Update, from surveys updates by the PIDS TWG, the 90 nm DRAM half-pitch began production ramp in 2005, on the completion of customer product qualification, which was made an explicit requirement of the "Production" definition for DRAM product for the 2003 ITRS.

Also based on the PIDS TWG surveys, the 2008 ITRS Table ORTC-1 DRAM product M1 half-pitch trend targets were calculated to align with an observed industry historical 2.5-year technology cycle (calculated from 180 nm/2000, 90 nm in 2005, and forecast to be 45 nm in 2010). Data provided by DRAM manufacturers suggests a three-year timing cycle (0.71× reduction) for DRAM stagger-contacted M1 half-pitch from the 2007/45 nm–2024/9 nm Roadmap period, as illustrated in Figure ORTC3.

Also mentioned above, the DRAM interconnect half-pitch will no longer continue to be used as a representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology cycle (0.71× reduction of the feature size). In fact, the Flash uncontacted polysilicon half-pitch feature continued on its 2-year cycle pace through 2010/32 nm, when it leads the DRAM M1 targets numerically by three years, and now is acknowledged by the Lithography ITWG to be the most leading driver of leading-edge technology manufacturing. Similarly, as mentioned, the lagging MPU and ASIC M1 stagger-contacted M1 interconnect half-pitches are running at a faster 2-year cycle pace and are presently expected to cross over the DRAM half-pitch in 2010/45 nm, and continue the 2-year pace through 2013/27 nm With the new product-oriented focus since the 2005 ITRS, all product technology trends will be monitored, and any of the product trends may accelerate further and begin to drive the industry research and the equipment and materials supplier development at the leading edge. See Figures 8a and 8b.

ROUNDED TREND NUMBERS

Using 180 nm DRAM product half pitch in the year 2000 as the calculation standard for trends, the 2011 ITRS includes an update of the past "rounding" convention for the technology cycle trend target. The actual calculated mathematical trend data (used for model calculations in the ORTC and TWG tables) reduces by 50% every other technology cycle, resulting in actual versus rounded number targets comparison below, starting from 350 nm in 1995, as follows in Table D.

Table D Rounded versus Actual Trend Numbers (DRAM Product Trend Example)

YEAR OF PRODUCTION	*1995*	*1998*	*2000*	*2002.5*	*2004*	*2005*	*2006*	*2007.5*
Calculated Trend Numbers (nm)	**360**	**255**	**180**	**127.3**	**103.4**	**90**	**68.2**	**63.6**
ITRS Rounded Numbers (nm)	**350**	**250**	**180**	**130**	**100**	**90**	**70**	**65**

YEAR OF PRODUCTION	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*	*2019*	*2022*	*2023*	*2024*	*2026*
Calculated Trend Numbers (nm)	**45**	**40.1**	**31.8**	**28.35**	**22.5**	**17.9**	**15.9**	**14.2**	**10.0**	**8.9**	**8.0**	**6.3**
ITRS Rounded Numbers (nm)	**45**	**40**	**32**	**28**	**22.5**	**17.9**	**15.9**	**14.2**	**10.0**	**8.9**	**8.0**	**6.3**

Note that the rounding corrections have become more critical as the industry moved into the two-digit data cycles of the nanotechnology (sub-100 nm) era. Please note also that some regions, for their own legacy publication consistency, will retain their right to continue to track the previous technology generations beginning with "100 nm"/2004. However, starting from "100 nm" in 2004, and using a 3-year cycle will result in "milestones" that are targeted to be close (within a year) to the present 2011 roadmap convention..

By consensus of the IRC, the unrounded number sets are available to the TWGs in the ORTC excel tables for long-term calculations, since the originalITRS long-term columns were retained (2009/45 nm; 2012/32 nm; 2015/22.5 nm;

2018/15.9), and interim columns (2010/40 nm; 2013/28 nm; 2016/20.0 nm; 2019/14.2 nm) are now annualized and included as columns. It was decided for the 2008 ITRS ORTC Update to include one decimal place of rounding accuracy after 2016 for the published Table ORTC-1 header technology trend line items. The 2011 ORTC tables are now available in excel table files at www.itrs.net; and even more decimal places of accuracy,calculated by the models, are available for the use of readers in those excel tables.

UPDATES TO THE ORTC

The MPU/hpASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM. As mentioned, the DRAM trend is accelerated 1 year to 2009/45 nm from the 2009 and 2010 versions, however the MPU/hpASIC M1 half-pitch remains unchanged on the lagging two-year cycle trend that crosses DRAM now in 2012/32 nm, and then continues to 2013/27 nm before it turns to a three-year cycle for the balance of the roadmap period.

The Flash product half-pitch continues to be defined as an uncontacted polysilicon half-pitch, and has also been revised from the 2009 and 2010 ITRS additions by continuing the two-year cycle trend through 2009/39 nm, but then accelerating to the 2010/24nm then turning to a 4-year cycle (0.5x per 8 years) through 2020/10 nm As mentioned above, at the 2020 point, the Flash trend is equal to the original 2009 and 2010 version target and returns to a 3-year pace to 2022/8nm; at which point, the trend remains flat to 2026/8nm due to anticipated Flash cell design limitations.. Refer to Figures ORTC3 and ORTC4. The Flash 3D bit layer model is a significant addition to the 2011 ORTC Flash Product technology trend tracking, and includes the trade-off with reduced poly uncontacted half pitch trends, along with the anticipated chip sizes and bit densities that result from the PIDS TWG models of that "equivalent scaling" technology tradeoff. Lithography masks count impact of the Flash 3D bit layers technology is discussed in an Executive Summary "*Lithography Masks Count special topic* and also in more detail in the PIDS chapter.

Due to trade-offs with "equivalent-scaling" process enhancements (copper and low-κ interconnect, strained silicon, high-K/Metal Gate, MugFETs, FDSOI, III/V Ge, etc.), as performance and power management alternatives (see Figure ORTC5), the *printed* MPU and *physical* gate length trends received major corrections in the 2008 and 2009 ITRS ORTC, which remain virtually unchanged in the 2011 ITRS. As described above, the physical gate length trend has been aligned with historical and survey data and is on a slower 3.8-year cycle trend beginning 2009/32 nm through 2024/7.5 nm. The printed gate length begins a delayed three-year cycle trend in 2011, and continues through 2026 on a "shrinking" ratio relationship to the physical gate length out to 2024/7.9 nm, just slightly larger than the expected final physical gate length at that time. Refer to Figure ORTC4. Due to recent announcements of production of MugFET technology in 2011 and possible acceleration of III/V Ge from 2019 to 2015 by a leading company, there will need to be significant work by the TWGs in the 2012 Updated to deal with the impact of the 4-5-year accelerations of those "equivalent scaling" technologies (see *Technology Pacing/Timing and Frequency/Power Executive Summary special topics*.

The dimensional and "equivalent scaling" technology accelerations are further evidence that the ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process will continue to provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2012 ITRS Update process, and the possibility of additional adjustments to the technology cycle in some of the individual product technology trends. As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future Roadmap trend shifts, it was agreed to continue the practice of publishing annual technology requirements from 2011 through 2018, called the "Near-term Years," and also annual requirements from 2019 through 2026, called the "Long-term years." As can be noted in Figures ORTC3 and ORTC4, the Long-term years of the 2011 ITRS are now somewhat aligned with the timing of the especially-challenging sub-1x nm technology era (2019/13-14nm M1 to 2026/6.3-6nm M1).

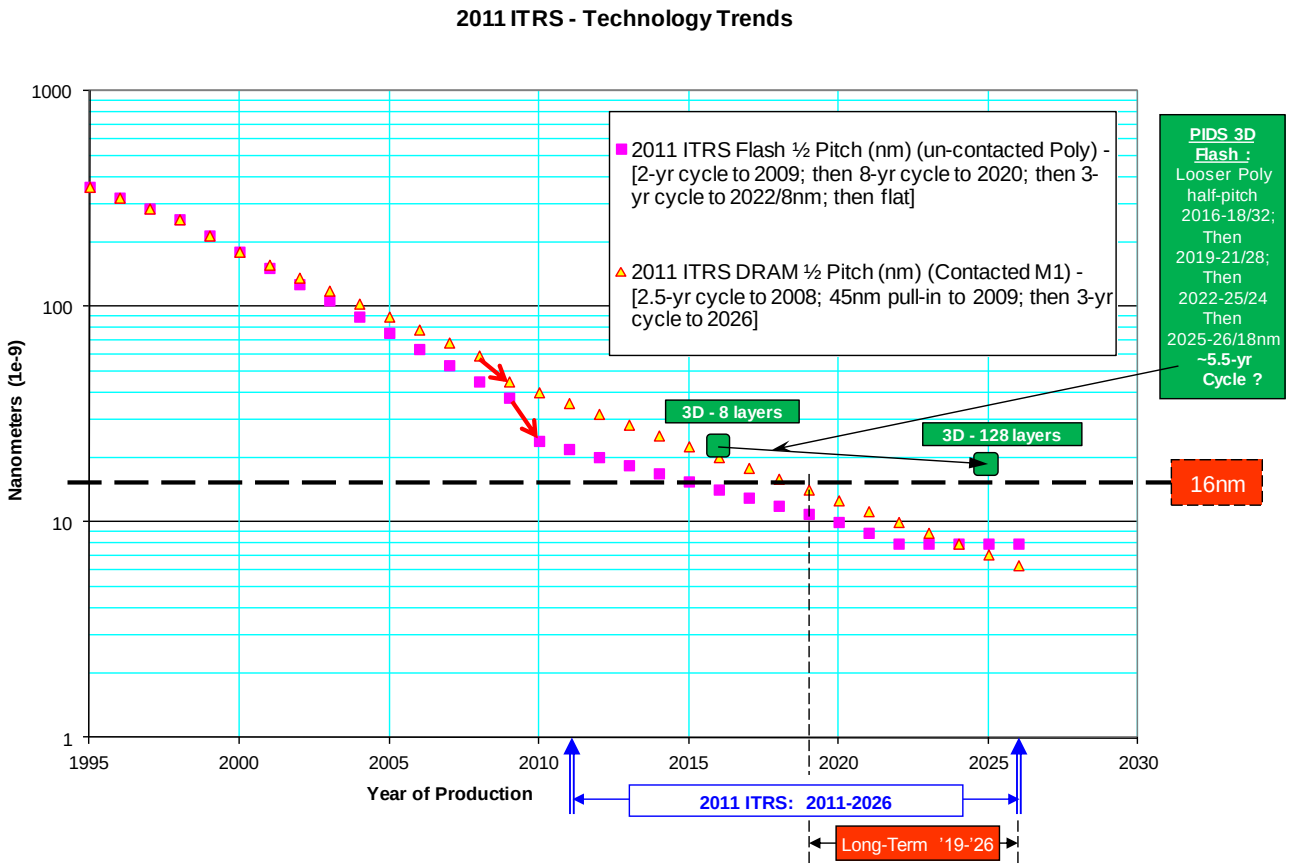


Figure ORTC3 *2011 ITRS—DRAM and Flash Memory Half Pitch Trends*

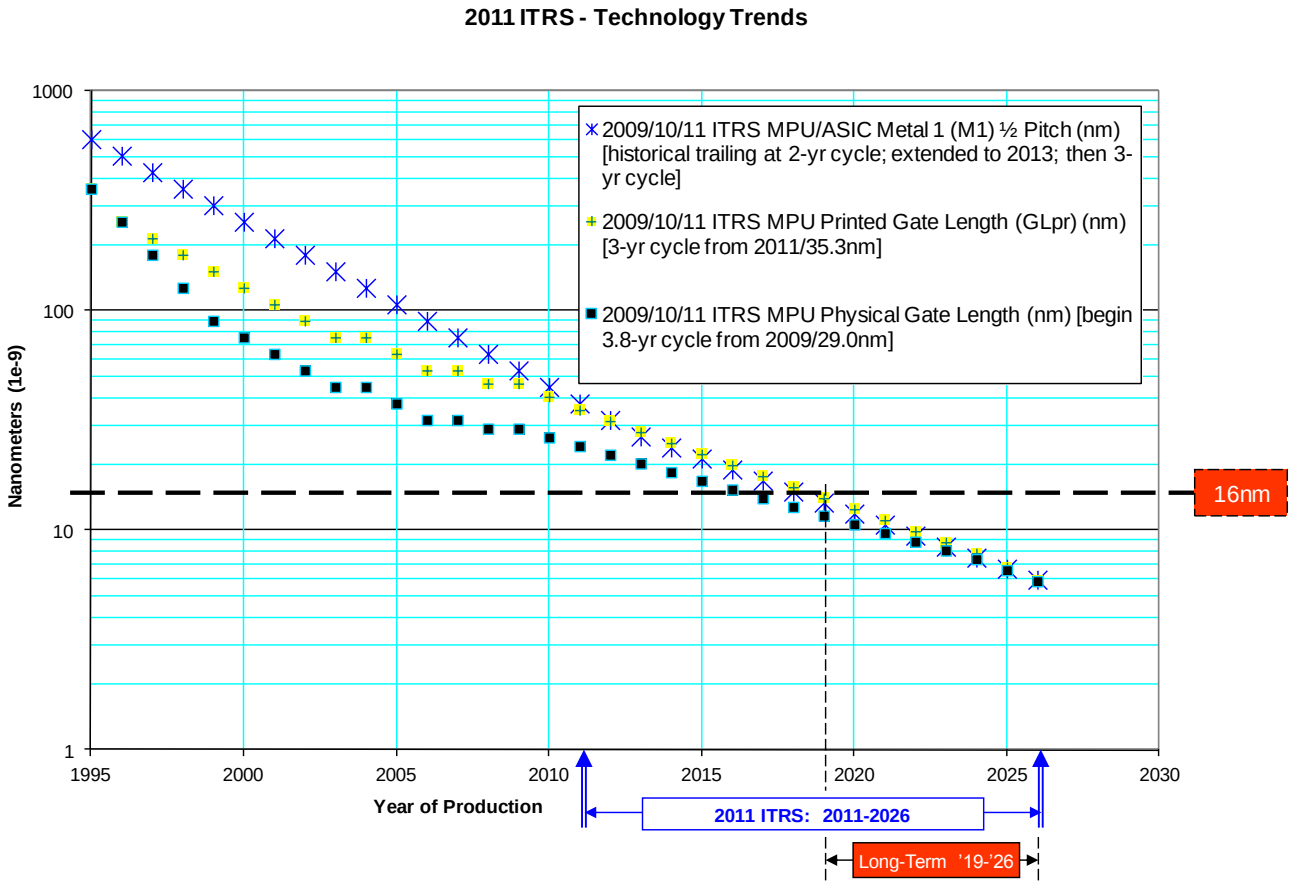


Figure ORTC4 *2011 ITRS—MPU/high-performance ASIC Half Pitch and Gate Length Trends*

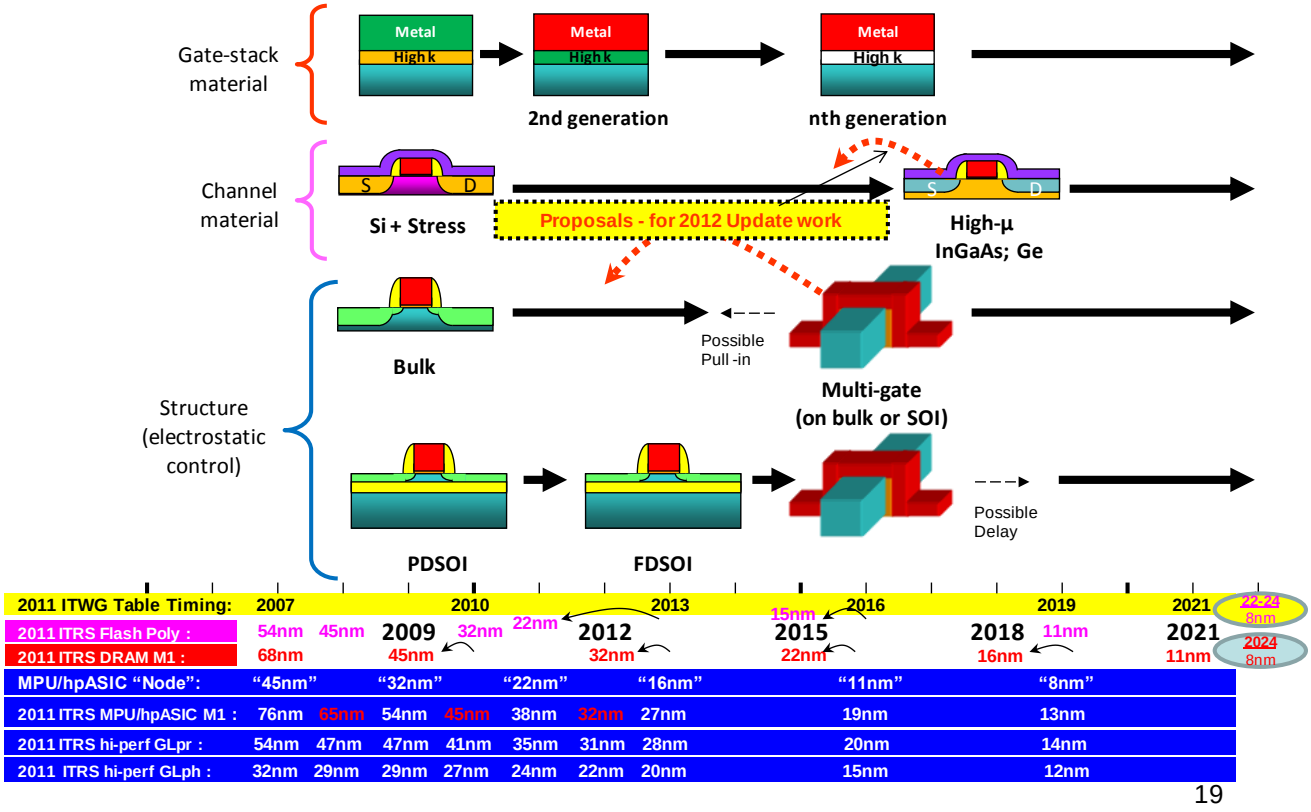


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Figure ORTC5 2011 ITRS "Equivalent Scaling" Process Technologies Timing compared to ORTC MPU/high-performance ASIC Half Pitch and Gate Length Trends and Timing and industry "node" naming; and including proposals for MugFET and III/V Ge acceleration for 2012 ITRS Update work; see PIDS, FEP, ERD, ERM chapters for additional details

PRODUCT GENERATIONS AND CHIP-SIZE MODEL

This section discusses "product generations" and their relationship to technology cycles, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology cycle timing advancement. Continuing a practice that began with the 2005 ITRS, the 2011 ITRS edition bases the technology pace drivers on individual product technology trends. These product-based technology trends may move on different paces from one another, based upon market functionality and performance and affordability needs, as the leading-edge product evolutions/shrink paths become more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the late-1990s, logic [as exemplified by MPU/high-performance ASIC (MPU/hpASIC)] technology moved at the same pace as DRAM technology, but lagged behind. The 2007 PIDS surveys of DRAM manufacturers concluded that after 2000/180 nm DRAM technology advancement was moving at an average 2.5-year. During the last few years, the development rate of new technologies used to manufacture MPU/hpASIC has continued on the 2-year pace, and is expected to continue on the 2-year pace through 2013/27 nm, while DRAM technology is presently forecast to accelerate 1 year and then return to the slower three-year cycle pace beginning 2009/45 nm through the 2026 Roadmap horizon. As mentioned, by moving on the faster 2-year cycle pace, MPU/hpASIC products are closing and even crossing the half-pitch technology gap with DRAM, and are expected, along with Flash technology needs, to drive the most leading-edge lithography tools and "equivalent-scaling" processes—especially for the capability to process and add power-management and performance enhancement characteristics to the isolated-line feature of the printed and physical gate length (such as etch-shaping, strained silicon, high-K/Metal Gate, MugFET, FDSOI, III/V Ge, etc.). As noted above, the Flash technology trend is defined by uncontacted polysilicon, and has also accelerated to the point where it is now driving at the most leading edge. As mentioned, the latest Flash technology also drives the most leading lithography and the PIDS

surveys forecast the Flash 2-year un-contacted poly half-pitch technology cycle pace to accelerate to 2010/24nm before turning to a 4-year cycle pace through 2020/10 nm; and is then on a 3-year pace to 2022/8nm, then flat to 2026/8nm due to anticipated Flash cell design limitations.

That being said, several fundamental differences exist between the families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore, development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch. The 2011 ITRS is now forecasting the insertion of new buried word and bit line cell technology, which will enable the $4f^2$ cell size, but delayed from the 2009 and 2010 ITRS versions to begin in 2013 (4=design factor and f=half-pitch in microns).

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length and "equivalent scaling" processes and design of the transistor gate, and also by the number and characteristics of interconnect layers and materials. The 2011 ITRS teams have reached consensus on models for the required functionality, chip size, cell area, and density for the updated ORTC tables. The MPU product chip size tables continue to be similar to the DRAM model, with large introductory chip sizes that must shrink over time to achieve the affordable sizes. Additional line items communicate the model consensus, and the underlying model assumptions are included in the ORTC table notations.

Table ORTC-1 [reference the ORTC excel tables, v8] summarizes the technology trend metrics mentioned above. For completeness, the ASIC/low power gate length trends are also included, and lag behind the high-performance MPU gate length targets in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of "equivalent-scaling," design factor, half-pitch, and gate-length features. For the DRAM product generations, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are included.

To summarize Figures ORTC3 and ORTC4, it should be noted that the long-term average annualized reduction rate of the DRAM contacted M1 half-pitch feature size is forecast to return to the three-year technology cycle pace after 2009/45 nm, which represents an approximately 11%/year (~30% reduction/three years). The previous (2000/180 nm–2008/52 nm) average 2.5year cycle rate is approximately 13%/year reduction on an annual basis (~24% reduction/two years). As noted above, the accelerated Flash memory uncontacted polysilicon is now expected to run at a slower 4-year pace and change back to the three-year pace in 2020; and will continue to leads both the DRAM M1. The MPU/hpASIC M1 until Flash technology levels to 8nm in 2026. As mentioned, the MPU/hpASIC product trends are generically referred to as MPU/ASIC in graphs, now crosses over the 1-year accelerated DRAM M1 in 2012/32 nm, and is forecast to continue on the two-year pace through 2013/27 nm before changing to a three-year pace.

Table ORTC-1 ITRS Technology Trend Targets

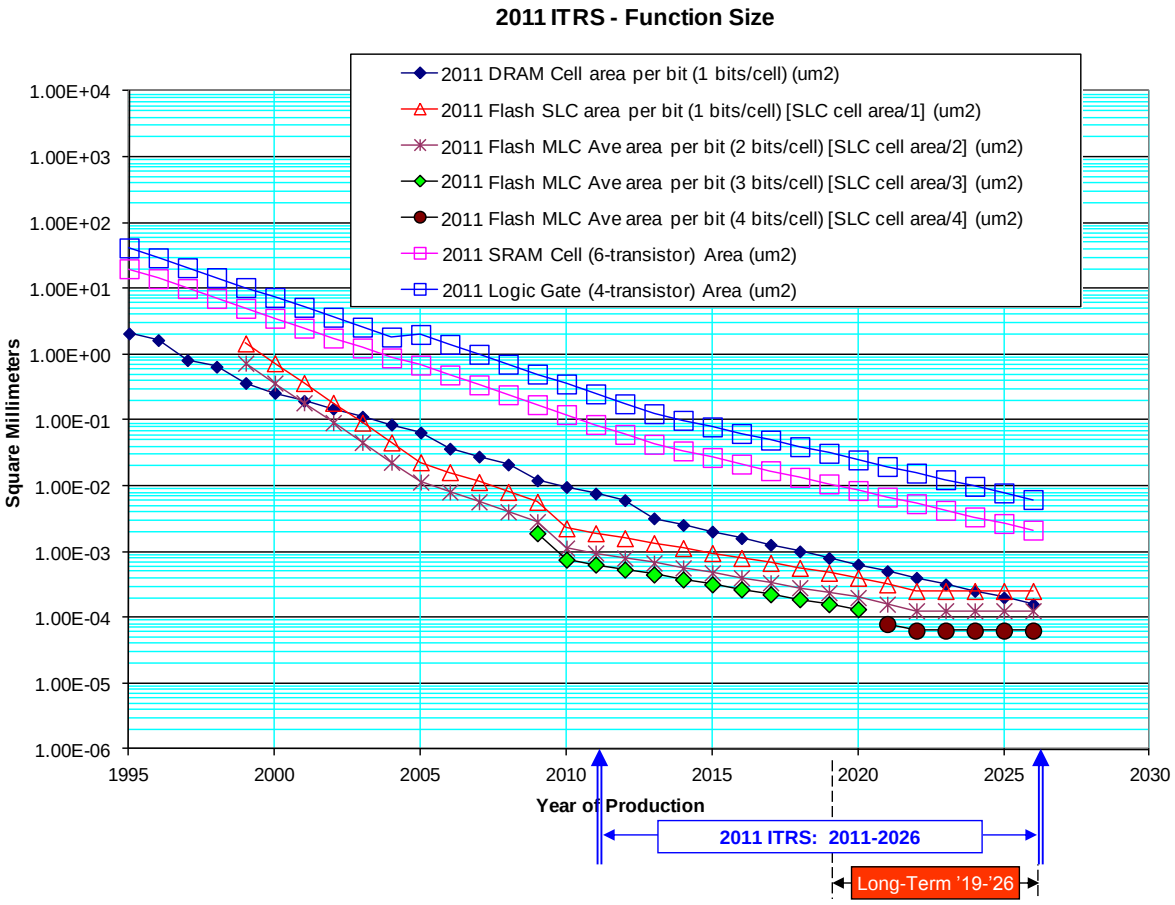

Figure ORTC6 2011 ITRS Product Function Size Trends: MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

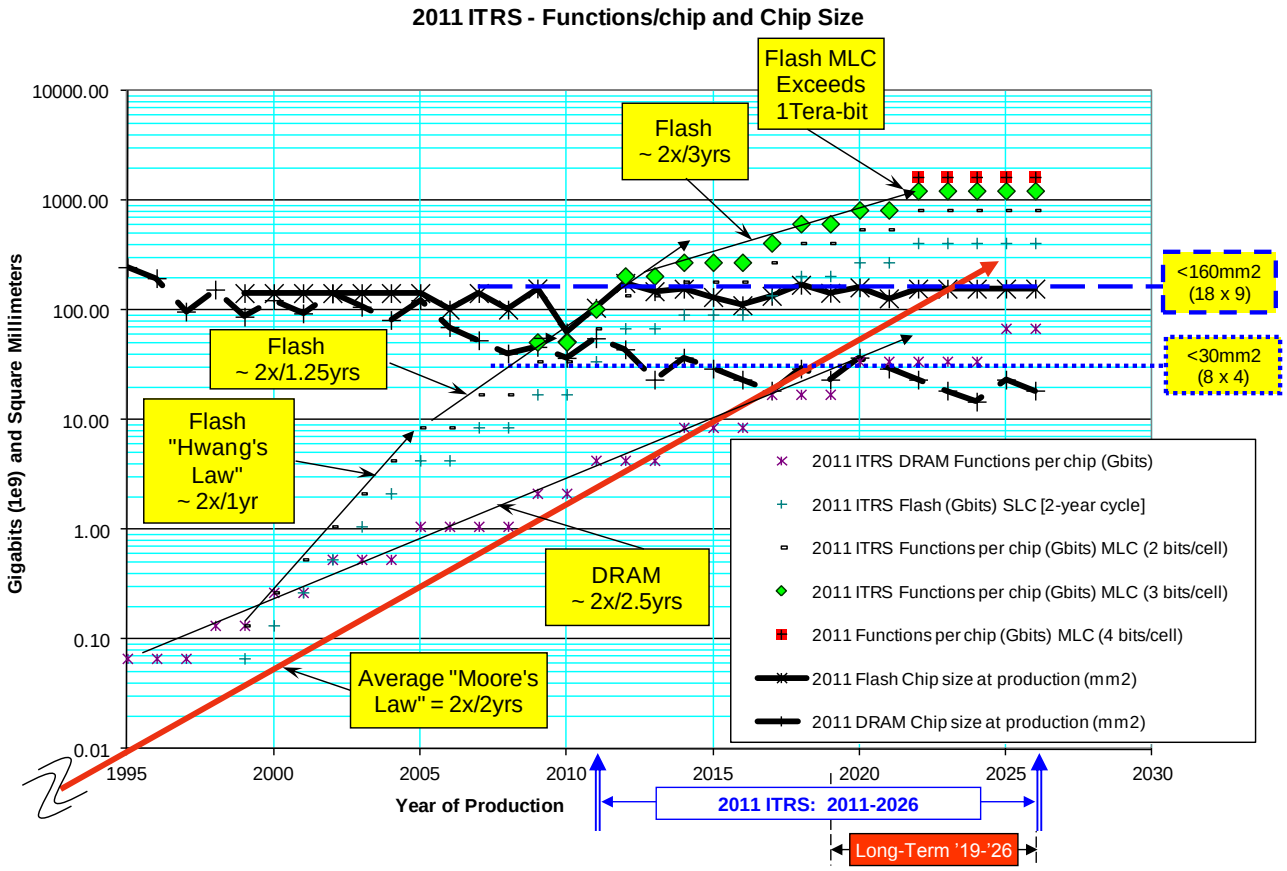

Figure ORTC7 2011 ITRS Product Technology Trends: Memory Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

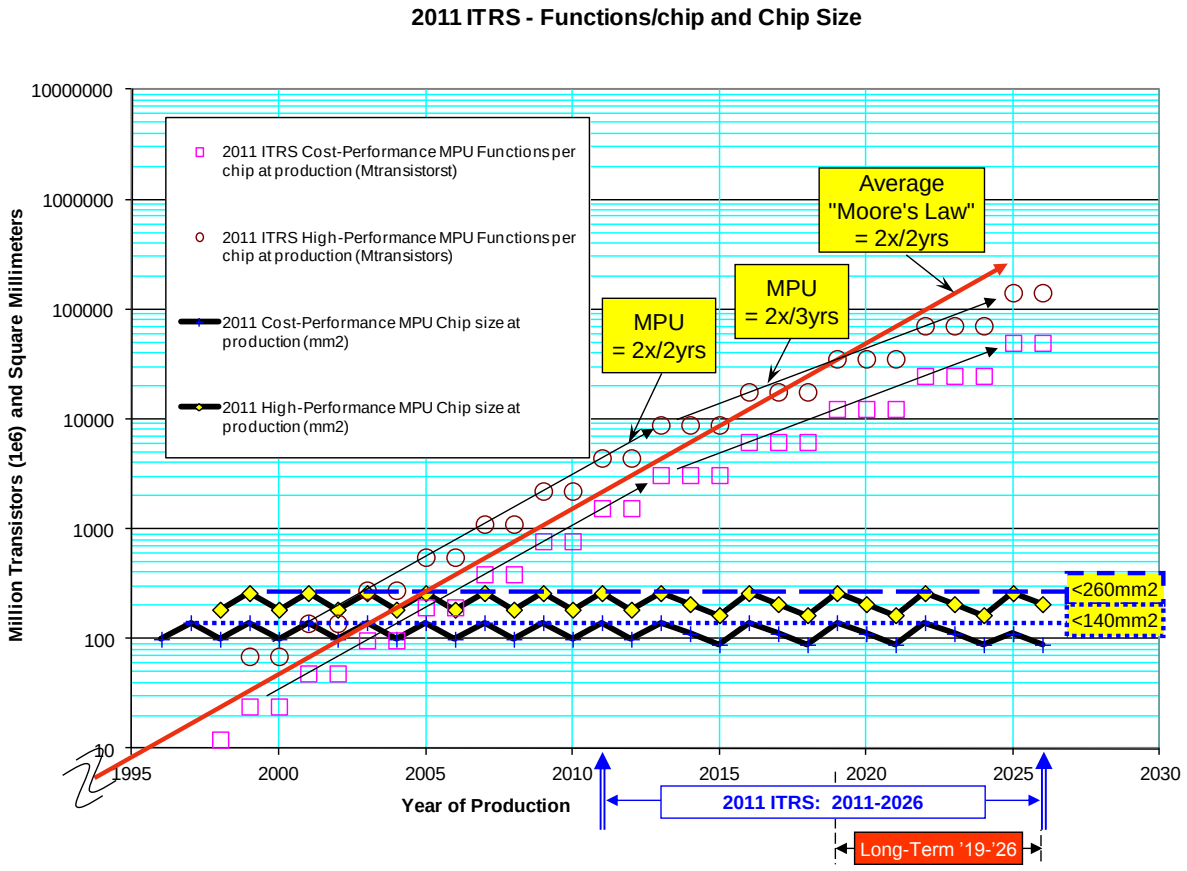

Figure ORTC8 2011 ITRS Product Technology Trends: MPU Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every two to three years, the chip size of first introductory-level leading-edge memory and logic product demonstrations in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) have continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 40%–60% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing the leading-edge product cost/function by ~30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, maintain or increase wafer and silicon area throughput, and, most of all, increase the number of functionality (transistors, bits, logic gates) and chips available on a wafer.

The increase in the gross number of functions and chips available on a wafer is primarily obtained by reducing the area of the functions and chips by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest ITRS product chip size models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must remain as flat as possible. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology cycle period, or faster when additional design-factor-related density improvement is available.

In order for affordable DRAM and Flash memory products to achieve virtually flat intra-generation chip-sizes, they must also maintain a cell area array efficiency ratio of 58–63% of total chip area. Historically, DRAM and Flash memory products have required reduction of cell area design factors (a) (cell area (Ca) in units of minimum-feature size (f) squared; $Ca = af^2$). The PIDS and FEP ITWGs have provided member survey data for the array efficiency targets, the

cell area factors, and bits per chip. In addition, detailed challenges and needs for solutions to meet the aggressive cell area goals are documented in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM and Flash memory cell area factors, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in Tables ORTC-2A and 2B. (Also refer to the Glossary for additional details).

Table ORTC-2A DRAM and Flash Production Product Generations and Chip Size Model

Table ORTC-2B DRAM Introduction Product Generations and Chip Size Model

Notably, the most recent survey data and publicly available announcements indicate that DRAM M1 contacted half-pitch trends have accelerated by one year and the reduction rate of DRAM cell area factors for the 2011 ITRS models place the $4f^2$ area factor in 2013 (versus 2011 area factor in the 2009/10 ITRS). Beginning 2013 the area factor is expected to remain flat at $4f^2$ through the 2026 ITRS horizon. In addition to the $4f^2$ factor change, the latest DRAM survey uses a 59% array efficiency from 2011 to the roadmap horizon in 2026. in the changes in DRAM half-pitch, cell design efficiency, and function density still enable lower targeted production chip sizes, which are now targeted for production sizes to be below 20 mm^2. Furthermore, the DRAM "Moore's Law" bits per chip targets continue to target 2× every three years in the near term, and delay by one year in and long term. The 64 Gbit DRAM product now sits at the ITRS year 2025 horizon.

In the updated 2011 ORTC Flash product model has been significantly revised. The function bit size is still calculated based upon the single-level cell (SLC) design factor and the also the critical feature scaling of the uncontacted polysilicon dense lines. The 2010 PIDS Flash survey indicated that the rapid 2-year scaling cycle now is expected to continue through 2009, but at 2010 the target accelerates 3 years to 24nm; however, the single-level-cell physical design factor limit remains at 4. Therefore, the Flash model function (bit size) area reduction has greatly accelerated, and the Flash uncontacted polysilicon half-pitch will continue to numerically lead the DRAM stagger-contacted M1 half-pitch by a wide margin; however the gap will reduce over time as the Flash survey expects a slower 4-year cycle (.5x/8years) until 2020/10 nm, at which point the trend returns to the original 2009/10 ITRS targets until 2022, when the trend levels at 8nm. The Lithography TWG continues to believe that leading-edge Flash manufacturing technology is clearly driving the most-leading-edge manufacturing, which also uses comparable processing equipment to manufacture leading-edge DRAM products.

Flash SLC bit technology was thus able to drive quickly to a 38 nm uncontacted polysilicon half-pitch and a "4" design factor in 2009; but now is expected to rapidly accelerate the scaling reduction to 24 nm in 2010, reducing SLC bit size to 0.0023 um^2 (nearly half the original 2009/10 ITRS target of 0.004um^2); and now one fifth the size of a DRAM cell that year (see Figure ORTC6, 2011 ITRS Product Function Size Trends). This continued acceleration of Flash technology will enable the production of a 106 mm^2 32 Gbit SLC product in 2011, when DRAM product is still at 4 Gbit (however, DRAM is only 56mm^2 to meet demanding market affordability and productivity requirements). Furthermore, Flash technology is able to create an electrical doubling of bits (multi-level-cell, or MLC) in the same area, resulting in a virtual doubling of bits per chip to 64 Gbits in the 106mm^2 affordable first production chip size range. The PIDS Flash survey added a three-bits-per-chip MLC product beginning 2009, and now extends 3bits per cell until 2020, delaying the more difficult quad-bit MLC to 2021 production.

The PIDS Flash table has now targeted 3D NAND cell layer technology to begin in 2016 with 8 layers stacked, but at a less demanding 32 nm uncontacted poly half-pitch technology. The PIDS model then adds addition layers through the roadmap range, with 128 layers at 18nm technology targeted for 2026. The slower technology pace is about a 5.5 year cycle, but the rapid addition of bit layers is expected to enable by 2025 an incredible SLC 2 Terabit device stacked on 128 layers on top of a 134mm2 base chip size. If 2bits/cell is used, the bits doubles to 4 Terabits in the same chip size. Due to its significance, the 3D NAND Flash technology has now been included in the ORTC Table 2a.

It is worthy of comment to the 2011 ITRS readers, that although a very large number of Flash technology processing steps and masks count are required (see the Litho Masks Count special topic), an analysis by commercial cost modeler IC Knowledge using ITRS-inspired process flows indicates that the cost/cm2 is very high, but the large number of bits added by multiple layers keeps the cost/bit trend on its historical reduction rate (contact ICK at www.icknowledge.com for additional information).

The ORTC MPU and High-Performance ASIC (hpASIC) models can remain unchanged in the 2011 ITRS Roadmap (except for extension to the 2026 horizon). This is due to the Design ITWG recommendations,in the 2008 and 2009 ITRS, the most dramatic changes since the 2001 ITRS. In the 2008-2009 editions, the Design ITWG had improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG added additional detail to the model, including new transistor design improvement factors. The new Design ITWG model utilizes a 60 design factor (significantly down from over 100 in previous roadmaps), in SRAM transistors, and is no longer expected to slowly improve over time. The logic gate transistor design factor was also dramatically reduced from over 300 to 175, and is also expected to remain flat throughout the roadmap period. Barring any significant changes in array efficiencies (the only other variable affecting the chip size models), the "shrink" and density improvements will continue to come from lithography-enabled interconnect half-pitch scaling.

The 2009 ITRS MPU model (used in both the 2010 and now the 2011 editions) ties to historical data by lagging an M1 half-pitch data trend on a two-year cycle trend, which now crosses over the DRAM M1 half-pitch in 2012/32 nm (due to the DRAM 1-year acceleration of 45 nm from 2010 to 2009, then continuing on a 3-year cycle through 2026), and then continues on the two-year cycle to 2013/27 nm before turning to a three-year cycle parallel to (and slightly smaller than) DRAM M1 half-pitch trend. MPU lags behind Flash uncontacted poly half-pitch numerically until the 2024 timeframe, when DRAM and MPU/hpASIC cross-over the flat 8nm target of Flash (Flash is expected to reach physics limitations that do not apply to DRAM and MPU/hpASIC). The technology dimension and design factor model was significantly revised in 2009 from past ITRS roadmaps, but still continues to reflect the competitive requirements for affordability by targeting flat chip size trends for both high-performance MPUs (now lowered to 260 mm^2) and cost-performance MPUs (still 140 mm^2).

Due to the MPU two-year-cycle half-pitch "catch-up-and cross-over phase" through the year 2013, the MPU products are targeted to maintain flat chip sizes due to lithography improvements alone. However, after 2013, the inter-generation MPU chip size model can remain flat only by slowing the rate of on-chip transistors to double every technology generation (3-year cycle after 2013).

In the 2011 ITRS, the MPU model continues to use the approach of doubling the logic cores only every other technology cycle. However, function size and density of the core was kept unchanged by doubling the transistors per core targets. The Design ITWG consensus opinion continues to maintain that this approach to the MPU Model is representative of current design trends. Refer to Function Size and Functions per Chip in Figures ORTC6, ORTC7, and ORTC8.

Due to the unchanged forecast extension of the MPU M1 half-pitch two-year technology cycle to 2013/27nm, the present MPU chip-size model can continue the historical Moore's Law doubling of on-chip functionality (transistors) until the 2013/27 nm point. After 2013, the Moore's Law rate of on-chip transistors slows to 2× every three years, to match the slower 3-year technology cycle (in order to maintain flat chip size targets). To keep the effective historical functional productivity on track after the 2013 point, MPU chip and process designers must add even more "equivalent scaling " design/process improvements to the designs to enhance the improvements provided by the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables ORTC-2C and 2D.

Table ORTC-2C MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model

Table ORTC-2D High-Performance MPU and ASIC Product Generations and Chip Size Model

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology to meet the demand for increasing maximum introduction-level chip sizes. The result was the achievement of very large step-and-scan fields (26×33 = 858 mm^2).

However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the Lithography ITWG limits the absolute maximum field size at 858 mm^2 and allows the individual memory and logic product chip size surveys and models to drive the requirements up to the absolute maximum field size and also the more typical affordable field size ranges.

DRAM chip sizes have historically been the driver of both the most difficult half-pitch exposures and also the affordable lithography field size range. In the 2011 ITRS chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than a 750 mm^2 lithography field size well under the 858mm^2 maximum, and fitting at least one introduction-level chip size within that field size. The latest 2011 ITRS production-level DRAM chip size model (less than 20 mm^2 new flat target) fits more than 29 die within a 572 mm^2 field.

The combination of technology generation scaling one-year acceleration, the higher array density, and cell design improvements (including the new $4f^2$ (placed in 2013 now) A-factor reduction) accomplishes that goal, while also allowing a goal of doubling on-chip bits to a slower 3-year cycle (and including a 1-year introduction delay in the long term). As mentioned in the product chip size model discussions above, the delay of the DRAM 4f2 design improvement to 2013, and the new under-20 mm2 affordable production chip size target, caused a requirement to add fewer on-chip bits in the long-term to stay under the affordable chip size and lithography field size. This was accomplished in the present DRAM model by delaying the production bits/chip generations by 1 year, and continuing the slower Moore's Law bits/chip rate at 2×/ three years to the end of the roadmap period. The data targets for the DRAM model are included in Tables ORTC-2A and 2B.

The Flash production chip size model is also included in those tables, and still targets the Flash maximum affordable chip size at under 150 mm^2, while continuing to target the doubling of Flash bits per chip every two years. Due to the extension of 2-year technology cycles to 2009for poly half pitch processing, the rapid acceleration in 2010 to 24nm poly half-pitch, plus the extension of 3bits/chip to 2020, when 4bits/chip multi-level cell (MLC) devices now appear, the Flash product chip sizes remain below 143mm^2 through 2026. The absolute maximum lithography field size is driven by the early introduction level chip sizes of high-performance MPUs and ASICs, which approach the maximum practical field size available from the Lithography TWG (26 × 33 = 858 mm^2). It is anticipated that future mask magnification levels as high as 8× may reduce the maximum field size to one-fourth the present 858 $mm^{2,}$ reducing the maximum available area to less than 214 mm^2. The details surrounding the limitations of maximum field size and the mask magnification issue are provided by the Lithography TWG in their chapter. The maximum Lithography field size targets are shown in Table ORTC-3, and are unchanged from the 2007 ITRS targets.

Table ORTC-3 Lithographic-Field and Wafer Size Trends

The 2011 ITRS DRAM, MPU and Flash models depend upon achieving the aggressive DRAM, MPU, and Flash design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industry's productivity-improvement and competitiveness.

With increasing cost-reduction pressures, the need for upgrading 200 mm manufacturing to 300 mm productivity boost (and also continuous improvement of the productivity of fabs) has increased in urgency more than ever, especially for leading-edge independent and foundry manufacturers. However, the poor economy, especially the most recent global recession, has created financial challenges and limited capital investment. The maximum substrate diameter in Table ORTC-3 (and in additional detail in the FEP chapter) is consistent with the ramp of 300 mm capacity, which began in 2001, and has now achieved 50 per cent of the industry silicon area capacity. Due to the expectation that 300 mm manufacturing technology admancement and continuous improvement would extend into the ITRS 2011 long-term (2019-2026), the decision was decided by the IRC extend the 300 mm manufacturing as a separate line item through the roadmap horizon of 2026.

The challenging economy has also affected the investment into, and the timing of, the incremental productivity boost expected from the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter (*as described in more detail in the 450 mm special topic section of the Executive Summary above)*. However, the availability of the 450 mm productivity boost continues to be targeted by the ITRS international roadmap committee (IRC) for integrated device manufacturer (IDM) and foundry pilot-line capability in the 2013-14 timeframe, based on ISMI progress reports, and announcements by leading companies which also target 2013-14 for pilot lines, and anticipate production ramps to happen in the 2015-2016 timeframe.

Other productivity-improvement drivers (lithography and design/process improvements) must also stay on schedule, as time is limited to accelerate the use of increased wafer diameter, or other equivalent processing solutions, to drive productivity improvement.

The effects of future technology acceleration/deceleration and the timing of the next wafer generation conversion require the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work continues to be sponsored and carried out jointly by Semiconductor Equipment and Materials International (SEMI) and SEMATECH, and now support from the commercial modeling sector is available from the ITRS-based IC Knowledge (www.icknowledge.com) Pre-competitive cooperation between the semiconductor supplier and manufacturer companies continues to be needed to define the future technical and economic needs and to identify appropriate funding mechanisms for the required research and development. Recent announcements of such cooperation are seen in the ongoing 450 mm program at SEMATECH; the new Global 450 mm Consortium (Intel, Samsung, TSMC, IBM, GlobalFoundries); and the European EEMI450 joint initiative with IMEC.

PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Table ORTC-4).

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. MPU and high-performance ASIC products approach 3–7K pads over the ITRS period. The MPU products are forecast to increase the total number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

Table ORTC-4 Performance and Packaged Chips Trends

Package pin count and cost-per-pin (Table ORTC-4), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow, while the cost/pin decreases. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually.

In the very competitive consumer electronics product environment (which is a focus end-product segment for characterizing Design and System-Driver Chapter Grand Challenges and Potential Solutions), prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases while the average cost per pin decreases, then: the average packaging share of total product cost will continue to increase over the 15-year roadmap period; and the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into systems-on-chip (SOC) and through the use of multi-chip modules (System-in-Package, i.e., SiP), bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double

every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. However, beginning in earlier roadmaps and continued in the latest 2011 ITRS, historical and forecast trends are suggesting a significant slowing in the rate of increase of on-chip frequency, to approximately only 4% growth per year or less (note additional comments below*). Performance increases accomplished historically by geometrical scaling (refer to Glossary) are now being provided through process "equivalent scaling" and also design-related "equivalent scaling" (see new definition updates in the Glossary) architecture and software improvements that enable the continued delivery of SOC, SIP, and system-level performance to customers while keeping power management under control.

For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational performance will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Table ORTC-4, which include line items contributed by the Design TWG to forecast the maximum on-chip trends. *During the 2011 ITRS work, the Design TWG examined the latest product data and trends, and proposed new On-Chip Clock Frequency targets on a 4% compound annual growth rate (CAGR) trend (versus the previou 2009/10 ITRS version trend of 8% CAGR, set during the 2008 ITRS work . The new frequency targets are significantly reduced from the previous targets, and will require additional 2012 Update work with the PIDs TWG to develop Intrinsic Transistor and Ring Oscillator models. This subject is dealt with in additional detail in the "*PIDS and Design Frequency" discussion in the Executive Summary Special Topic section.*

The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay and power usage is caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation and power dissipation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package.

To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip – see the A&P chapter and Interconnect Chapter for additional details).

LITHOGRAPHY MASKS COUNT AND ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Table ORTC-5. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 2 for DRAM and microprocessors. In addition, the data in the table are reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology by using the formula found in the Yield Enhancement chapter.

The estimates of the approximate number of masks count for logic and memory devices is included as an indicator of the ever-increasing process complexity, and work was accomplished in 2011 by the Lithography TWG to survey companies and revise the targets for the 2011 ITRS. .The ORCT Table 5 now includes line items from the Lithography survey and additional masks count modeling data contributed from the IC Knowledge (ICK) Strategic Model (based on the ITRS at www.itrs.net). More details on this significant 2011 ITRS work can be read in the *Executive Summary Special Topic, "Lithography Masks Count"* section.

Additional work must be done by the Yield Enhancement (YE) TWG in the 2012 Update to analyze and include a Defect Model update to the YE Do line items in ORTC Table 5.

Table ORTC-5 Lithography Masks Count and Electrical Defects

POWER SUPPLY AND POWER DISSIPATION

The reduction of power supply voltage is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Table 6, the value of the power supply voltage is now given as a specific target, rather than a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} below 0.6 volts are now target for high-performance processors by 2025. The lowest V_{dd} target is 0..54V in 2026 for the low operating power applications., Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable (low-cost, hand-held) battery operations. In all cases, total power consumption targets are relatively flat in the 2011 Table ORTC-6, despite the use of a lower supply voltage. The power consumption is driven by higher chip operating frequencies, the higher interconnect overall capacitance and resistance, and the increasing gate leakage of exponentially growing and scaled on-chip transistors.

The approach for calculating maximum power targets is being re-evaluated in the 2012 roadmap update calculation models from the Design and Assembly and Packaging (A&P) ITWGs are expected to take into account specific "hot-spot" area calculations rather than the overall chip area.

Table ORTC-6 Power Supply and Power Dissipation

COST

Table ORTC-7 is dedicated to cost trends. The historical ability to reduce the leading-edge product manufacturing cost per function by an average 29% each year (0.5× per 2 years) has represented one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this market cost reduction mandate, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with an approximately constant cost per cm2 of silicon. This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's challenging economic and competitive market environment continue to resist even moderate increases in per unit cost, maintaining the pressure upon the semiconductor industry to slow the rate of doubling functions per chip (Moore's Law) in order to keep chip and unit costs under control. The semiconductor manufacturers had to seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at constant cost targets. The 2001 and 2003, 2005, 2007, 2009 and now the 2011 ITRS models *all continue to use that idealized and simplistic model*, which results in 29% cost reduction of a function (bit, transistor, etc.). Note that the 29% average rate of function cost reduction was achieved historically (prior to 1999) by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The 2011 ITRS DRAM and MPU cost models continue to use the need for that average 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of 0.66 microcents for DRAMs in 2011. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in cost/bit should be expected.[5] A corresponding analysis conducted from published data for microprocessors provides

[5] *McClean, William J., ed. Mid-Term 1994: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1994.*
McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1995.

similar results.[6] Therefore, the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model, along with the 45%/year reduction rate within the same generation.

The 2011 ITRS has kept the MPU chip size model unchanged from the 2009 and 2010 versions. The Design ITWG had updated the MPU model in the 2009 ITRS, based upon their most recent available data and models. The new data and model indicate that logic transistor size is improving at the rate of the lithography (0.7× linear, 0.5× area reduction every technology cycle). Therefore, in order to keep the MPU chip sizes flat to the 140 mm2 target, the number of transistors can be doubled only every technology cycle. The technology cycle rate is projected to be on a 2-year cycle through 45 nm/2010, and turn to a three-year cycle after 2010. Therefore the transistors per MPU chip can double only every three years after 2013, unless increased chip size is allowed for specific applications which have markets that can afford the higher costs.

DRAM memory bit cell design improvements is expected to accelerate, as reflected in the 2011 ITRS DRAM Chip Size Model targets (see Table ORTC-2). In conjunction with the 1-year technology trend pull-in, the "4" design factor, a 33% improvement over the "6" factor, is now expected to be implemented in 2013, maintaining on avarage the long-range cost-reduction productivity. Furthermore, the latest PIDS TWG survey of DRAM manufacturers has indicated that the new higher target for the cell array efficiency percentage of 59% is expected to continue through the roadmap horizon, 2026. The recent model changes, along with the new goal of a more affordable starting production chip size (less than 60 mm2) have enabled the near-term bits/chip to remain unchanged. However the long-term bits/chip has been delayed by one year as a trade-off for even smaller and affordable chip sizes. The increase rate of bits per chip continues at 2×/3 years in the near term (2011/4G; 2014/8G) and stretches to 2x/3.5 years in the long term (2018/16G; 2025/64G). These DRAM model changes have pushed the 64 Gbit generation (introduction in 2013) to 2025 for production and the 128 Gbit DRAM (introduction 2014) remains beyond even the present 2026 ITRS horizon. .

To compensate for slowing DRAM and MPU (after 2013) functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the "equivalent" productivity scaling benefits of chip, package, board, and system-level architecture and designs.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This issue is reflected in the escalating cost of testers. The number of tested pins (see Table ORTC4) is also increasing, which adds to the cost of the tester as well as the associated material and custom test fixtures that increase the total cost of ownership. Therefore, there will be an ongoing need for accelerated implementation of built-in-self-test and design-for-testability and design-for-manufacturability techniques within the time frame of the 2011 ITRS. Further discussion is detailed in the Test and Test Equipment chapter.

Table ORTC-7 Cost

[6] *a) Dataquest Incorporated. x86 Market: Detailed Forecast, Assumptions, and Trends. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. Business Week, December 9, 1996, 148–152.

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
    - Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function)

integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets.

MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

As defined above, additional "Equivalent Scaling" process technologies can be combined with transistor gate dimensional scaling technology advancement to further advance the performance and power-management characteristics of a device. The "Equivalent Scaling" technologies can also be "mix-and-matched" by companies within their specific product fabs. In some cases the most recent ITRS TWG surveys have indicated that dimensional scaling (both gate length and gate material thickness) reduction can be slowed and still meet power management and performance requirements, when traded off with "equivalent scaling" process insertion.

Some (not comprehensive or complete) examples of "equivalent scaling" process and transistor design technology are: copper interconnect; low-K interconnect materials; strained silicon; high-K/metal gate; fully depleted silicon-on-insulator (FDSOI); multiple-gate 3-D transistors, III-V gate material; etc.

It should be noted that the timing of availability and implementation of "equivalent scaling" process insertion may not be as regular as dimensional cycles. See the Interconnect and process integration and device structures (PIDS) chapters for additional technology description and timing details.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to the "Moore's Law" driver of functions/chip doubling every two years , there has been a historically-based "corollary" to the "law," which suggests that, to be affordable and competitive, manufacturing productivity improvements must also enable the cost-per-function (micro-cents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 2 years, cost per function must also reduce by half every 2 years (-29%/year average). On average then cost-per-chip (packaged unit) , for affordability, could remain approximately constant (requires both flat chip cost targets and flat back-end packaging targets to remain constant), If functionality doubles only every three years, then the manufacturing cost per chip (packaged unit) can remain flat if the cost per function reduction rate slows to one-half every 3 years.(-21%/year average). It should be noted that this simplistic manufacturing cost affordability model, used as a first-order driver for the ITRS, does not take into account the economic supply and demand market complexity of actual external market environments.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two to four bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two and level-three (L2 and L3) cache. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation.

High-performance MPU[7]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores with large level-two and level-3 (L2 and L3) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory. Recently the typical pattern among MPU products is to keep the number of cores constant within a generation and double the number of transistors within each core, and the latest ITRS ORTC modeling reflects this trend in the table targets.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still maintained, although the latest consensus ITRS forecast of cell-area-factor improvement to 4 by 2011, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate. Therefore, the latest ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The latest ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2005 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (typically <1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition,

[7] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, 10K/month or higher, depending upon die size and wafer generation size) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2a in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: .5 Gb/production, 4 G/introduction, plus 256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2009 ITRS, the typical high-performance ASIC (hpASIC) design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 74% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 56% at the production level, and also for shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C=Af^2=0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=74% of total chip area, the $C_{AVE} = C/E = 0.35\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.35e-6 mm^2/bit = 376 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two to four bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half to one-fourth the size of an SLC product cell size and will also have a "virtual area factor" that is half to one-fourth of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 10–15 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2–3 times greater than an SRAM 6t cell area factor, and 30–40 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities. Additional clarification was added by the IRC in 2009 to differentiate the new 450 mm wafer generation early consortia pilot line equipment readiness from the timing of anticipated production readiness and ramp.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.