2009 ITRS ORTC
Technology Trends
[from Taiwan Public Conference and online Exec. Summary at www.itrs.net]

For the IEEE Santa Clara Chapter Special Topic, Tues, 03/16/10
National Semiconductor Site

Allan - Rev 0, 03/16/10

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Agenda

- History/Background
- Pre-Summary
- Moore's Law and More
- Technology Pacing Trends Update
- Some TWG Highlights
- 2009 ITRS 450mm Timing Update
- Summary

- Backup

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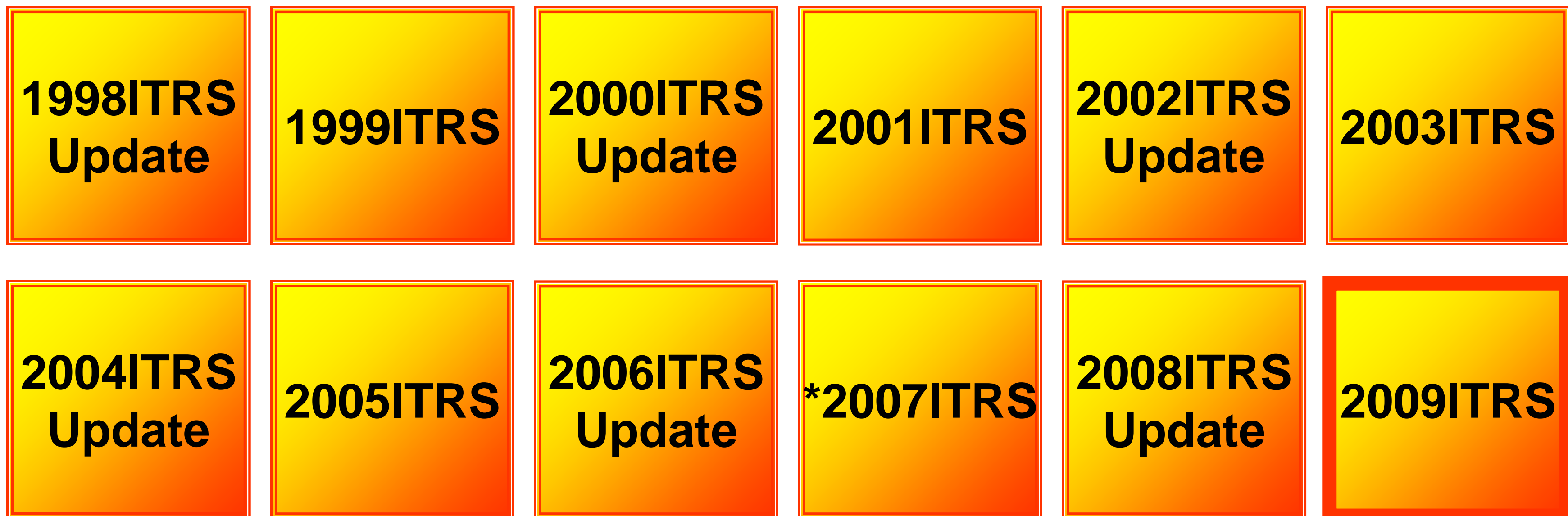
2007-08 - 10th Anniversary of ITRS!

http://www.itrs.net [*incl. Public Presentations]

Europe Japan Korea Taiwan USA



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2009 ITRS ORTC (pre-)Summary

1) ORTC Model Completed and delivered to TWGs for TWG Interdependency Preparation
   1) MPU Model completed based upon Design TWG model proposals
   2) Memory Chip Size and density models complete based on Brussels proposal presentation by PIDS
   3) Some new features:
      1) "Beyond CMOS" timing added for ERD/ERM early research and transfer to PIDS
      2) "Equivalent Scaling" Timing updated and compared to "Dimensional" Trends
      3) "More than Moore" white paper to be added [in 2010] to ITRS website at www.itrs.net
2) MPU M1 Update
   1) 2-year cycle trend added and extended through 2013
   2) Cross-over DRAM M1 2010/45nm
   3) Plus Smaller $60f^2$ Design TWG SRAM 6t cell Design Factor
   4) Plus Smaller $175f^2$ still proposed Logic Gate 4t Design Factor
3) DRAM M1
   1) Dimensional M1 half-pitch trends unchanged from 2007/08 ITRS
   2) However, new 4f2 Design factor begins 2011
4) Flash Un-contacted Poly – extended 2yr cycle trend to 2010/32nm (1-year pull-in); then 3yr cycle and also added "equivalent scaling" bit design:
   1) Inserted 3bits/cell MLC 2009-11; and
   2) Delayed 4bits/cell (2 companies in production) until 2012

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2009 ITRS ORTC (pre-)Summary (cont.)

5) MPU GLpr – ’08-’09 2-yr flat; Low operating and standby line items track changes
6) MPU GLph – ’08-’09 2-yr flat with equiv. scaling process tradeoffs; Low operating and standby line items track changes
   1) Performance targets (speed, power) on track with tradeoffs
7) MPU Functions/Chip and Chip Size Models
   1) Utilized Design TWG Model for Chip Size and Density Model trends – tied to technology cycle timing trends and updated cell design factors
   2) High Performance MPU Transistors/chip crosses DRAM bits/chip in 2009 at 2Bt/2Gbits!
   3) ORTC line item added to deal with OverHead (OH) area model changes to deal with non-active area
8) DRAM Bits/Chip and Chip Size Model
   1) 1-yr push-out, 3yr generation “Moore’s Law” doubling cycle;
   2) smaller Chip Sizes (<60mm2) with 4f2 design factor included
9) Flash Bits/Chip and Chip Size Model
   1) 1-yr pull-in; 2yr generation “Moore’s Law” doubling cycle;
   2) growing Chip Sizes after return to 3-year technology cycle
   3) PIDS Scenario option proposal (for 2010 Update work): “mix and match” 2yr and 3yr doubling cycles across SLC and MLC products
10) New IRC 450mm Position: Pilot lines/2012; Production/2014-16
   1) New “double S-curve” graphic added to Executive Summary to clarify

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2009 ITRS Update Highlights (pre-)Summary (cont.)

Some ITRS TWG Chapter Highlights (more at www.itrs.net)

- Design and System Driver Continue to Provide More Roadmap Detail and Framework for Application Needs and cross-TWG "equiv. scaling" Potential Solutions
- Litho Technology Potential Solution options Cost of Ownership Tradeoff
- PIDS tables adapted to new ORTC trends, plus Transistor "equivalent scaling" Modeling Developed for Performance and Power Options
- ERD/ERM workshops underway to prioritize "Beyond CMOS" "information processing" potential solutions, including next storage element
- A&P New Categories and TSV focus on accelerating 3D SIP and 3D Interconnect implementations
- FI – focus on productivity improvement through systematic waste reduction
- Additional Details Available in Online Roadmaps and Public Presentations at www.itrs.net ; incl. linked Future Fab 2009 ITRS special edition articles

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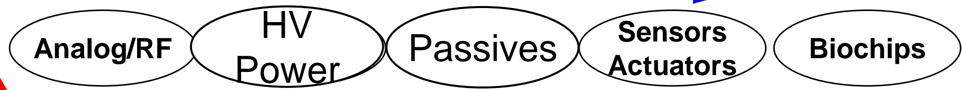
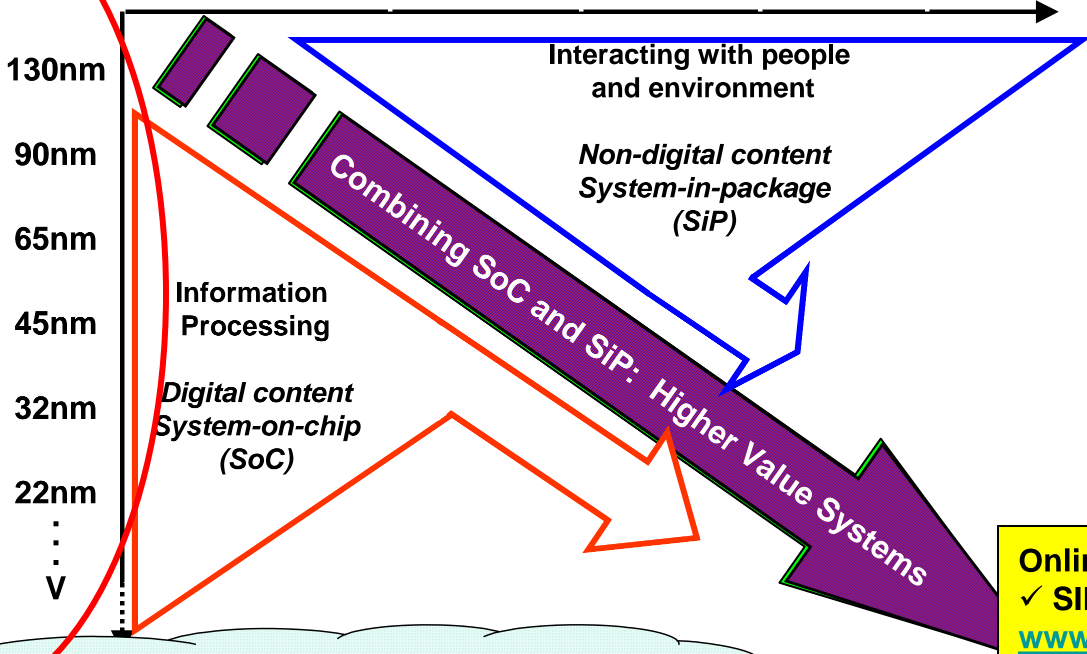
2007 ITRS Executive Summary Fig 4

Moore's Law & More

✓New work In 2009

Traditional ORTC Models





New in 2009:
- ✓ More than Moore "White Paper"
- ✓ More Commentary In ITWG Chapters

New in 2009:
- ✓ Survey updates to ORTC Models
- ✓ Equivalent Scaling Roadmap Timing Synchronized with PIDS and FEP

Online in 2008:
- ✓ SIP "White Paper" www.itrs.net/papers.html

New in 2009:
- ✓ Research and PIDS transfer timing clarified
- ✓ Work underway to identify next storage element

Source: 2009 ITRS - Executive Summary Fig 1

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ITRS Definitions - "Moore's Law and More"

Below are the "ITRS-approved definitions" from the 2009 Executive Summary Glossary online at www.itrs.net; http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_ExecSum.pdf :

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

PLEASE NOTE THAT THE 2009 ITRS GLOSSARY INCLUDES NEW DEFINITION ADDITIONS AND UPDATES.

Moore's Law—

[Is] An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- ***Geometrical*** *(constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- ***Equivalent Scaling*** *(occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- ***Design Equivalent Scaling*** *(occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
  - o "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
  - o Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—

The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

Design technologies enable new functionality that takes advantage of More than Moore technologies. "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology." Addresses the need for design technologies which enable functional diversification

Beyond CMOS—

Emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions ["new storage element" to be developed in the 2010 and 2011 ERD/ERM work].

Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

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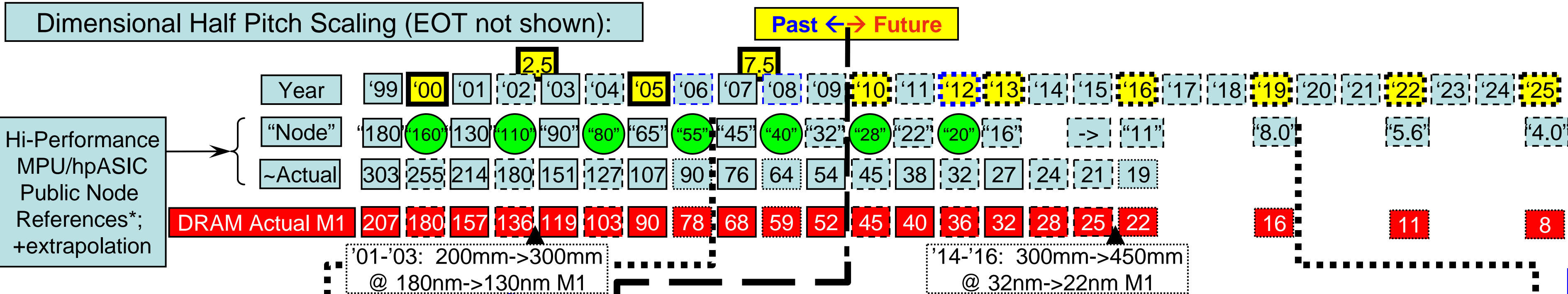
Industry "Node"* Alignment w/ITRS

DRAM Density "Equiv. Scaling":	8f²	8f²	6f²	4f²	TBD	TBD	TBD
Flash Density MLC "Equiv. Scaling":	16/11/8/5.5/4f2: 2b/cell	2.0f²: 2b/cell		1.5f²: 3b/cell	1.0f²:4b/cell TBD	TBD	TBD
MPU Perform/Power "Equiv. Scaling":	Copper	Strain	HiK/MG I, II	FDSOI	MUGFET; SiGE	III/V Hi-u	TBD



Past ↔ Future

"Node" vs M1 and Poly Alignment

2009 ITWG Table Timing:	2007			2010			2013	2016	2019]
2009 IS ITRS Flash Poly :	54nm	45nm		32nm			22nm	16nm	11nm
2009 IS ITRS DRAM M1 :	68nm			45nm			32nm	22nm	16nm
MPU/hpASIC "Node*":	"45nm"		"32nm"		"22nm"		"16nm"	"11nm"	"8nm"
2009 ITRS MPU/hpASIC M1 :	76nm	65nm	54nm	45nm	38nm	32nm	27nm	19nm	13nm
2009 ITRS hi-perf GLpr :	54nm	47nm	47nm	41nm	35nm	31nm	28nm	20nm	14nm
2009 ITRS hi-perf GLph :	32nm	29nm	29nm	27nm	24nm	22nm	20nm	15nm	12nm

2009 ITRS: 2009-2024

*Notes on "Nodes": DRAM, Flash "Nodes" ~= M1 and Poly Half-pitch.
However high performance Logic (MPU, hpASIC) may have node "labels" Associated with their dimensional technology progress, as referenced in:

1) MPU reference: Mark Bohr Tutorial, Jul'09: http://www.wesrch.com/Documents/view_editorial.php?flag=3&editorial_id=EL1FYLN

2) hpASIC reference TSMC "Nodes" Articles: http://www.xbitlabs.com/news/other/display/20080930205529_TSMC_Unveils_32nm_28nm_Process_Technologies_Roadmap.html ; http://www.eetimes.com/news/semi/showArticle.jhtml?articleID=177100620

MPU & ASIC Low-Power versions typically lag Gate Length to manage power and performance trade-offs at the same M1-based density "Node" as high-performance versions

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"Equivalent Scaling Process Technologies Timing"

New for 2009

[PIDS/FEP – "Simplified Transistor Roadmap"] - [Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs (ENIAC Graphic)]

Gate stack

poly / SiON → metal / high k → metal / high k [II, etc]

['09: 2 co's (1st co: 2007)]

['11: 2 co's (1st co: 2009)]

Electrostatic control

bulk → MuGFET MuCFET

PDSOI → FDSOI → MuGFET MuCFET

Channel material

stressors → + high μ SiGe materials → + III/V High μ Alternative Channel Mat'ls

2009 ITWG Table Timing: 2007 2010 2013 2016 2019]

Source: 2009 ITRS - Exec. Summary Fig 7c

[Orig. Source: ITRS, European Nanoelectronics Initiative Advisory Council] (ENIAC)

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2009 – Updated add ERD/ERM Research and PIDS Transfer

Production Ramp-up Model and Technology Cycle Timing

Source: 2009 ITRS - Exec. Summary Fig 2a

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ERD/ERM Long-Range R&D and PIDS Transfer Timing Model Technology Cycle Timing

[Example: III-V MOSFET High-mobility Channel Replacement Materials]

New for 2009

Research | Development | Production

Transfer to PIDS/FEP (96-72mo Leadtime)

Alpha Tool | Beta Tool | Product Tool

First Tech. Conf. Device Papers Up to ~12yrs Prior to Product

First Tech. Conf. Circuits Papers Up to ~ 5yrs Prior to Product

1st 2 Co's Reach Product

Volume (Wafers/Month): 200K, 20K, 2K, 200, 20, 2

Months: -96, -72, -48, -24, 0, 24

III/V Hi-μ gate Example:

2011 | 2013 | 2015 | 2017 | 2019 | 2021

Source: 2009 ITRS - Executive Summary Fig 2b

Work in Progress – Do Not Publish!

Including '11 snapshot Analysis

Figure 7a

2009 ITRS - Technology Trends

Memory

* http://www10.edacafe.com/nbc/articles/view_article.php?section=ICNews&articleid=794291

*..Samsung..begun mass producing the industry's first low-power (green) four gigabit (Gb) DDR3 devices using 40 nanometer (nm) class process technology…]

■ 2009 ITRS Flash ½ Pitch (nm) (un-contacted Poly) - [2-yr cycle to 2010; then 3-yr cycle]

△ 2009 ITRS DRAM ½ Pitch (nm) (contacted) [2.5yr cycle '00-'10, then 3-yr cycle]

2011
ORTC Targets
DRAM
40nm M1
Flash
28nm
Poly(uncont.)

16nm

Nanometers (1e-9)

1000
100
10
1

1995
2000
2005
2010
2015
2020
2025

Year of Production

Near-Term

Long-Term

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 7a

Work in Progress – Do Not Publish!

Including '11 snapshot Analysis

Figure 7b

2009 ITRS - Technology Trends

Logic

1000

100

10

1

Nanometers (1e-9)

1995 2000 2005 2010 2015 2020 2025

Year of Production

2009 ITRS MPU/ASIC Metal 1 (M1) ½ Pitch (nm) [historical trailing at 2-yr cycle; extended to 2013; then 3-yr cycle]

2009 ITRS MPU Printed Gate Length (GLpr) (nm) [3-yr cycle from 2011/35.3nm]

2009 ITRS MPU Physical Gate Length (nm) [begin 3.8-yr cycle from 2009/29.0nm]

2011
ORTC Targets
"22nm"
(38nm M1)
GLpr 35nm
GLph 24nm

16nm

Near-Term

Long-Term

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 7b

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Including survey input Analysis

Figure 8

Function Size

Memory & Logic

- 2009 DRAM Cell area per bit (1 bits/cell) (um2)
- 2009 Flash SLC area per bit (1 bits/cell) [SLC cell area/1] (um2)
- 2009 Flash MLC Ave area per bit (2 bits/cell) [SLC cell area/2] (um2)
- 2009 Flash MLC Ave area per bit (3 bits/cell) [SLC cell area/3] (um2)
- 2009 Flash MLC Ave area per bit (4 bits/cell) [SLC cell area/4] (um2)
- 2009 SRAM Cell (6-transistor) Area (um2)
- 2009 Logic Gate (4-transistor) Area (um2)

MPU/ASIC Alignment With Latest Design TWG Actual SRAM [$60f^2$] & Logic Gate [$175f^2$]

DRAM $4f^2$ Added Beginning 2011

Flash [$4f^2$]
1) 2-yr Cycle Extended to 2010;
2) 3 bits/cell added 2009-2011;
3) 4 bits/cell moved To 2012

Square Micrometers (um2): 1.00E+04, 1.00E+03, 1.00E+02, 1.00E+01, 1.00E+00, 1.00E-01, 1.00E-02, 1.00E-03, 1.00E-04, 1.00E-05, 1.00E-06

Year of Production: 1995, 2000, 2005, 2010, 2015, 2020, 2025

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 8

Work in Progress – Do Not Publish!

Including '11 snapshot Analysis

Figure 9a

2009 ITRS - Functions/chip and Chip Size

Memory

* http://www10.edacafe.com/nbc/articles/view_article.php?section=ICNews&articleid=794291

*..Samsung..begun mass producing the industry's first low-power (green) four gigabit (Gb) DDR3 devices using 40 nanometer (nm) class process technology…]

2011:
DRAM 40nm; Flash/28nm
Model Bits/chip Generations

Flash SLC
1 Tera-bit!

Flash
= 2x/2yrs

<143mm2
(22 x 6.5)

<60mm2
(11 x 5.5)

DRAM
= 2x/3yrs

Flash
"Hwang's
Law"
= 2x/1yr

DRAM
= 2x/2yrs

Average "Moore's Law" = 2x/2yrs

Gigabits (1e9) and Square Millimeters

10000.00
1000.00
100.00
10.00
1.00
0.10
0.01

1995 2000 2005 2010 2015 2020 2025

Year of Production

- 2009 ITRS DRAM Functions per chip (Gbits)
- 2009 ITRS Flash (Gbits) SLC [2-year cycle]
- 2009 ITRS Functions per chip (Gbits) MLC (2 bits/cell)
- 2009 ITRS Functions per chip (Gbits) MLC (3 bits/cell) ADDED
- 2009 Functions per chip (Gbits) MLC (4 bits/cell)
- 2009 Flash Chip size at production (mm2)
- 2009 DRAM Chip size at production (mm2)

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 9a

Work in Progress – Do Not Publish!

Including '11 snapshot Analysis

Figure 9b

2009 ITRS - Functions/chip and Chip Size

Logic

10000000
1000000
100000
10000
1000
100
10

Million Transistors (1e6) and Square Millimeters

2009 ITRS Cost-Performance MPU Functions per chip at production (Mtransistorst)

2009 ITRS High-Performance MPU Functions per chip at production (Mtransistors)

2009 Cost-Performance MPU Chip size at production (mm2)

2009 High-Performance MPU Chip size at production (mm2)

* http://www.intel.com/technology/architecture-silicon/2billion.htm

*[Next-generation Intel® Itanium® processors (codenamed Tukwila).. processor-based server technology..As the world's first 2-billion transistor microprocessor.. targeted for production in Q1 2010..]

Average "Moore's Law" = 2x/2yrs

MPU = 2x/3yrs

MPU = 2x/2yrs

2011: "22nm"/(38nm M1) MPU Model Generations

<260mm2

<140mm2

1995 2000 2005 2010 2015 2020 2025

Year of Production

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 9b

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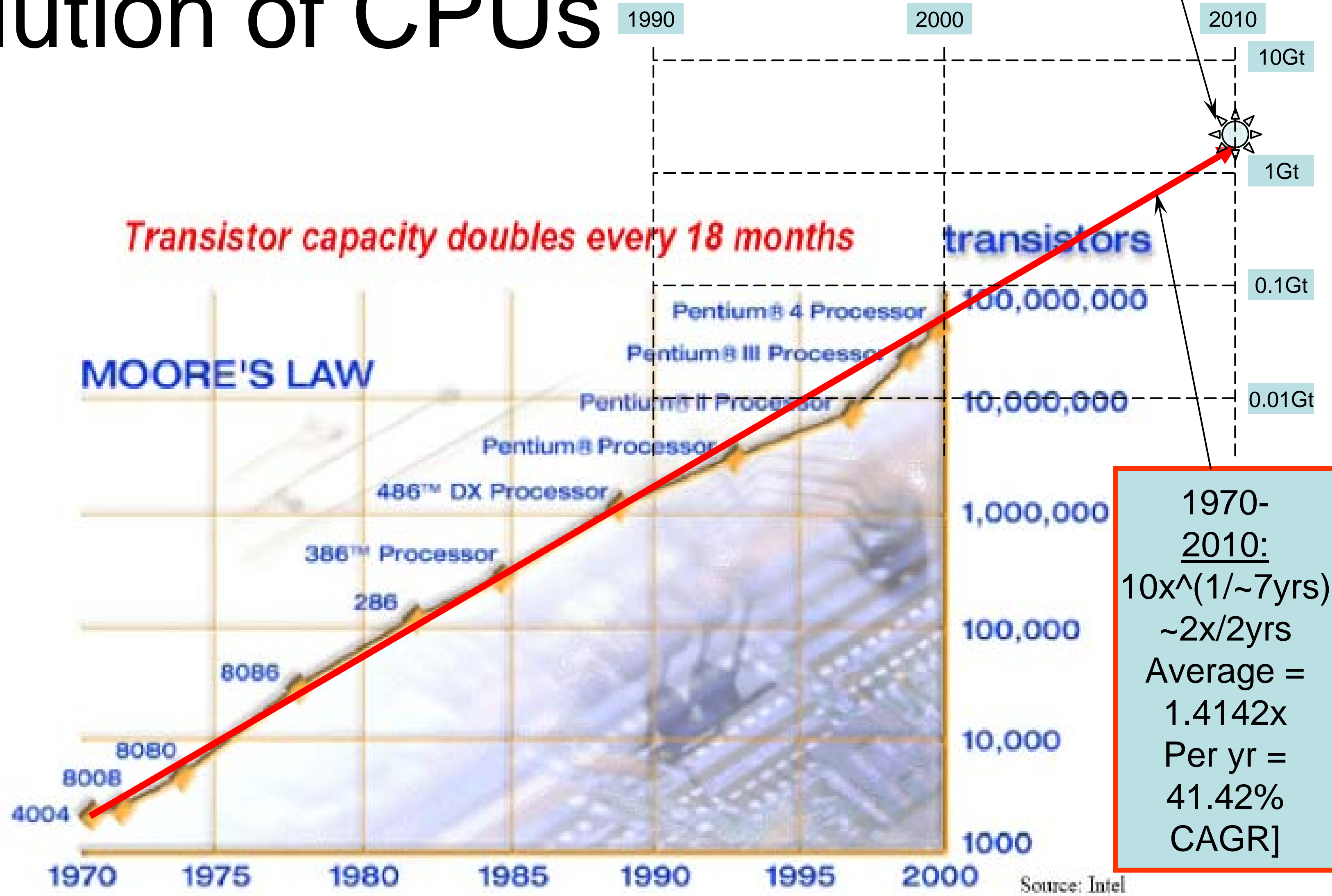
Evolution of CPUs



Source: http://www.sonoma.edu/users/f/farahman/sonoma/courses/es310/Lectures/Chapter1.ppt#317,20,Evolution%20of%20CPUs

In 1965, Gordon Moore, co-founder of Intel, indicated that the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented. Moore predicted that this trend would continue for the foreseeable future.

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Some Selected ITWG Chapter Highlights

- Design and System Drivers
- Litho
- PIDS
- ERD
- A&P
- FI
- Exec Summary 450mm “Special Topic”
- See rest and much more at www.itrs.net

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2009 Design & System Drivers ITWGs

Design

1. **Software, system level design productivity critical to roadmap**
2. **Initiated reliability / resilience roadmap**
3. **System-level design technology is key to power efficiency**
4. **Design cost will be contained through innovation**

System Drivers

1. **Design update to ORTC: SRAM, logic, defect density models**
2. **Updated key system drivers: SOC-Consumer Portable, MPU**
3. **Frequency-power envelope remains critical for industry**
4. **Updated System Drivers, no new drivers**
5. **Expanded cross-TWG and public activity (DAC '09 workshop)**

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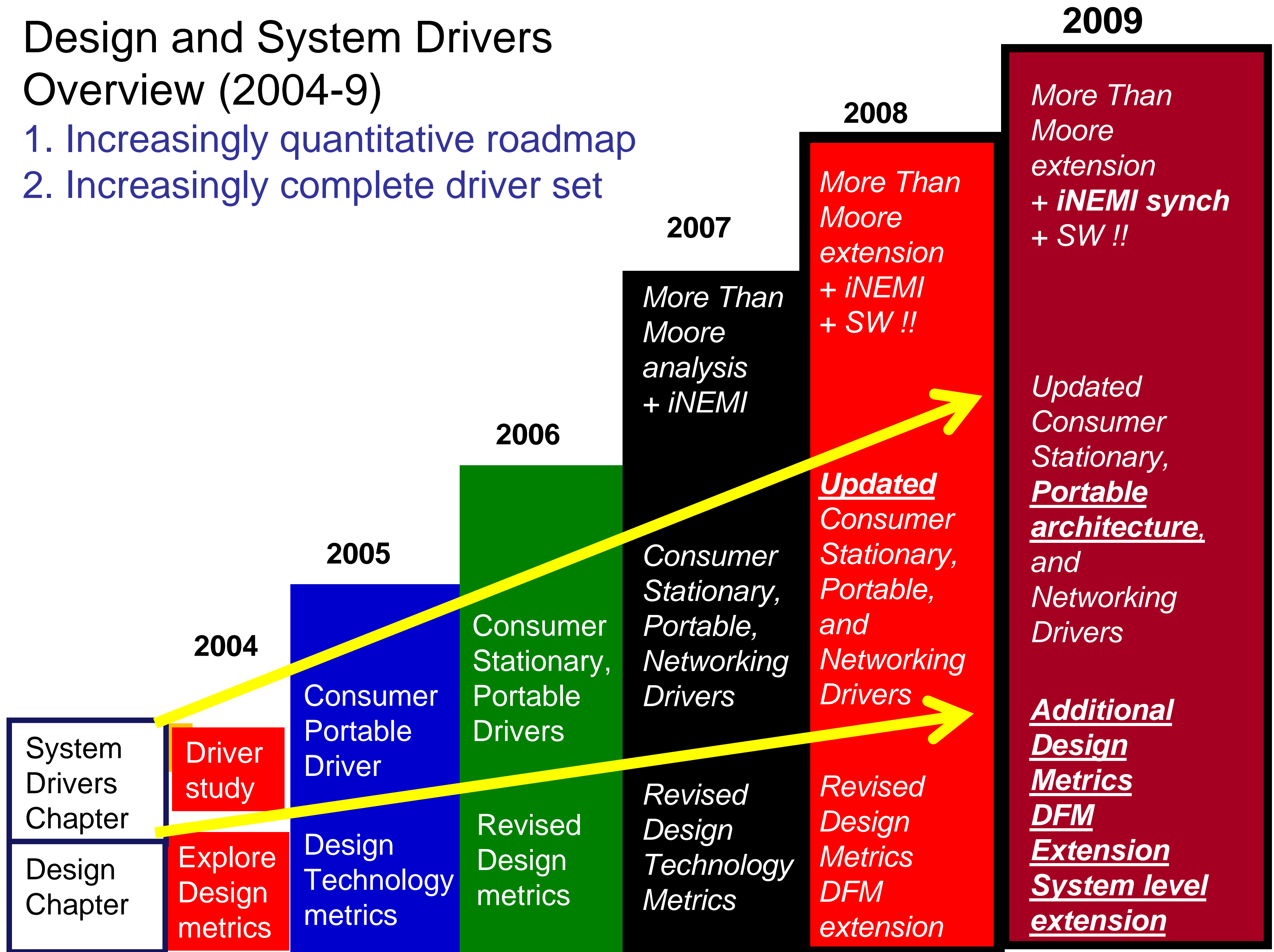
Design and System Drivers Overview (2004-9)
1. Increasingly quantitative roadmap
2. Increasingly complete driver set
2004
2005
2006
2007
2008
2009
System Drivers Chapter
Design Chapter
Driver study
Explore Design metrics
Consumer Portable Driver
Design Technology metrics
Consumer Stationary, Portable Drivers
Revised Design metrics
More Than Moore analysis + iNEMI
Consumer Stationary, Portable, Networking Drivers
Revised Design Technology Metrics
More Than Moore extension + iNEMI + SW !!
Updated Consumer Stationary, Portable, and Networking Drivers
Revised Design Metrics DFM extension
More Than Moore extension + iNEMI synch + SW !!
Updated Consumer Stationary, Portable architecture, and Networking Drivers
Additional Design Metrics DFM Extension System level extension

2009 Litho

- Lithography solutions for 2010
  - 45 nm half-pitch CoO is Driving 193 Immersion Single Exposure for DRAM/MPU
  - Flash using Double Patterning (Spacer) for 32 nm half-pitch
- Lithography solutions for 2013
  - 32 nm half-pitch Double patterning or EUV? for DRAM/MPU
  - 22 nm half-pitch Double patterning or EUV for Flash
- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single layers
- LER and CD Control Still remain as a Dominant Issue
- Mask Complexity for Double patterning
- Mask Infrastructure for EUV

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Litho Potential Solutions

	First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
	DRAM ½ pitch (nm) (contacted)	*52*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	38	32	28	25	23	20	18	16	14	13	11	10	8.9
45	**193 nm immersion with water**													
32	**193 nm Immersion Double Pattern**	Narrow Options												
	EUV (DRAM / MPU)													
22	**EUV**													
	193 nm Immersion Double / Multiple Pattern			Narrow Options										
	ML2													
	Imprint													
		No proven optical solution below this line												
16	**EUV**													
	Innovative 193nm immersion Multiple Pattern													
	ML2						Narrow Options							
	Imprint													
	Directed Self Assembly													
	Interference Lithography													
11	**EUV**													
	ML2													
	Imprint									Narrow Options				
	Directed Self Assembly													
	Interference Lithography													

MPU / DRAM time line

Flash Time Line

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Litho Potential Solutions Cost of Ownership Tradeoff

Cost of Ownership for 5000 wafers per mask

Reticle Cost
Other
Resist Cost
Consumable Cost
Capital Cost

Double Patterning

EUV

65 DP Dry
65 SE-NA 1.35
45nm DP (125 wph)
45nm SE (125 wph)
32nm DE (90 wph)
32nm Line DP (180 wph)
32nm EUV (100 wph)
22nm Line TP (200 wph)
22nm EUV (100 wph)

Figure 2. The Relative Cost of Ownership for the Critical Level of a 5000-Wafer Run Device vs. Lithography Process and Node

2009 PIDS

Logic

- Ring-oscillator delay added. Fan-out = 1 and 4.
- I_{sat} of *p*-MOSFET added. Other parameters assumed symmetric.
- Subthreshold currents held constant independent of L_{gate}/year. HP, LOP, LSTP = 100 nA/µm, 5 nA/µm, 50 pA/µm respectively.
- Criterion for S/D parasitic resistance set for degradation of 33%.

DRAM

- Small cell factor–$4F^2$ introduced in 2011.
- DRAM product size 1 yr delay from ITRS 2007/2008 (4 Gb in 2011).

NVM

- Floating-gate to charge-trapping NAND flash transition in 2012, delay 2 yr.
- 3 bit/cell – 4bit/cell transition delays 2 years, to 2012.
- 3-D charge-trapping flash in 2014, delay 1 year.
- STT (spin-torque-transfer) MRAM added.

Reliability

- Major revisions in the reliability requirement specifications.

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2009 ERD

- Process for Technology Transfer to PIDS/FEP made explicit
- Logic Devices
  - New Logic Table structure defined to identify three device categories
    (1 – Extend CMOS; 2 – Charge-based Non-CMOS; 3 – Non-charge-based Beyond-CMOS)
  - New potential solution table for "Carbon-based Nanoelectronics"
- Memory Devices
  - Transfer Engineered Tunnel Barrier Memory to PIDS/FEP
  - A new taxonomy for categorizing resistive memories introduced.
  - An assessment of new memory devices is underway
  - STTRAM and Nano-wire PCM scaled beyond 15nm
- Architecture
  - New Architectural work for benchmarking "Beyond CMOS" devices is underway
  - New Memory Architecture section includes 1) memory architecture. 2) a new inference compute proposal, and 3) a conceptual thermodynamic method for evaluating architecture.

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Evolution of Extended CMOS

Elements

More Than Moore Elements

More Than Moore

More Moore

Top-down

Bottom-up

Beyond CMOS

Beyond CMOS Elements

Extended CMOS

ERD-WG in Japan

Beyond CMOS

year

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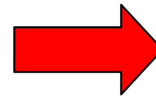
A&P 2009
Revision made to single chip package categories

Previous Categories
Low-cost/hand held
Cost performance
High performance
Harsh



New Categories
Low-end, Low-cost
Mobile/Handheld
Memory
Cost performance
High performance
Harsh

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A&P - Tera-scale Computing by 2015

TSV die to die connection

Silicon Interposer with:
-Integrated thermal management
-Integrated Passive networks

200GB; 500GB/s memory
(20 sectors at 25GB/s)

Memory cube
1Tbyte; 500GB/s
(20 sectors at 25GB/s)

Memory
Memory
Memory
Interposer
Memory
Memory
Memory
Interposer
Memory
Memory
Memory
Memory

Memory
Memory
Interposer
Processor
Processor
Interposer
Processor
Processor
Interposer
Processor
Processor
Interposer
Processor
Processor
Interposer
Processor
Processor

Optical channel

System in Package Substrate
With CNT based heat spreader

1TB/s optical transceiver for:
- Off package communication
- On package routing

Processor with 1000 cores/10 layers
Core transistor speed 1GHz
25um thick wafer (~400mV power)

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2009 Factory Integration

- Mission changeover
  - 200➔300mm driver ➔NGF
  - More FO service oriented requirements
  - Less physical requirements except for 450mm
- FI proposes Waste Reduction drive in ITRS
  - In parallel with Si Scaling
  - Encouragement through cross TWG activity
  - Plan Waste Reduction as roadmap at each TWG
- Systematic productivity improvement
  - Systematic waste reduction by systematic PDCA cycle execution as NGF enabler
  - Proactive visualization
  - FI set up 2 waste metrics
- 2010 and after
  - More on waste reduction
    - Seek for acceptance by other ITWGs and needed FO services
  - Green Initiative implementation
    - Need energy saving waste management metrics
  - Systematic restructuring of Potential Solution

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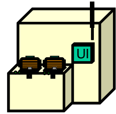
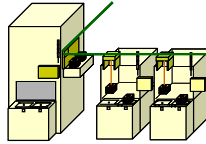
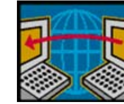
FI Focus on Wafer Manufacturing

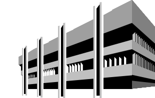
FITWG Thrust Teams

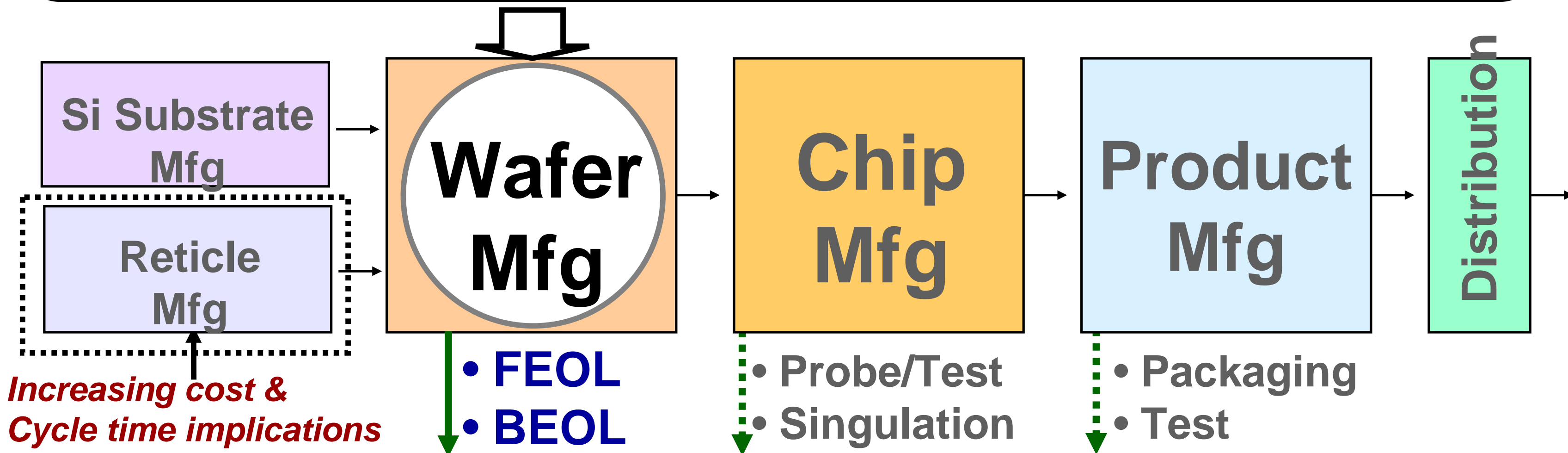
Factory Operations


Production Equipment


AMHS


Factory Information & Control Systems


Facilities



Factory is driven by Cost, Quality, Productivity, Speed, and Flexibility

- Reduce factory capital and operating costs per function
- Faster delivery of new and volume products to the end customer
- Efficient/Effective volume/mix production, high reliability, & high equipment reuse
- Enable rapid process technology shrinks as well as systematic productivity waste reduction

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2009 ITRS 450mm Update

[from Public ORTC San Francisco SEMICON, July, 2009]

ITRS IRC 2009 Position (Source 2009 Executive summary; 450mm Special Topic):

"….Intel, Samsung, and TSMC (IST) announced in May'08 that they will work together with suppliers, other semiconductor players and ISMI to develop 450mm with a goal of a pilot line in 2012. Full production may be 2-3 years after that[1]. This Public announcement and assessment may be subject to revision based on future statements; but it is the statement of record by these three companies and ISMI, as of the date of writing of the ITRS 2009 edition

The timing of the production ramp of 450 mm facilities (versus early pilot line capability) depends not only on the mastering of all technical issues, associated with this transition to a new diameter, but also on the preparedness of the industry. To assess the likelihood of that timing, the whole value chain must therefore be examined…"

"…Furthermore, and new in the 2009 ITRS, a 450mm Production Ramp-up Model Graphic has been provided (Figure 2c) to clarify the special dual "S-curve" timing required when a new wafer generation is being introduced [modeled after the experience with the 300mm wafer generation ramp on two succeeding technology cycles in the 2001-2003 (180nm-130nm M1) timeframe]…."

[1] Source: "May 2008"/ "Oct 2008 ISMI symposium"/Dec'08 ISMI 450mm Transition Program Status Update for ITRS IRC, Seoul, Korea [and also at SEMICON Japan]

2009 ITRS WORK IN PROGRESS – DO NOT PUBLISH

New for 2009

450mm Production Ramp-up Model

[2009 Figure 2c A Typical Wafer Generation Pilot Line and Production "Ramp" Curve]

Source: 2009 ITRS - Executive Summary Fig 2c

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2009 ITRS ORTC Summary

1) ORTC Model Completed and delivered to TWGs for TWG Interdependency Preparation
   1) MPU Model completed based upon Design TWG model proposals
   2) Memory Chip Size and density models complete based on Brussels proposal presentation by PIDS
   3) Some new features:
      1) “Beyond CMOS” timing added for ERD/ERM early research and transfer to PIDS
      2) “Equivalent Scaling” Timing updated and compared to “Dimensional” Trends
      3) “More than Moore” white paper to be added [in 2010] to ITRS website at www.itrs.net
2) MPU M1 Update
   1) 2-year cycle trend added and extended through 2013
   2) Cross-over DRAM M1 2010/45nm
   3) Plus Smaller $60f^2$ Design TWG SRAM 6t cell Design Factor
   4) Plus Smaller $175f^2$ still proposed Logic Gate 4t Design Factor
3) DRAM M1
   1) Dimensional M1 half-pitch trends unchanged from 2007/08 ITRS
   2) However, new 4f2 Design factor begins 2011
4) Flash Un-contacted Poly – extended 2yr cycle trend to 2010/32nm (1-year pull-in); then 3yr cycle and also added “equivalent scaling” bit design:
   1) Inserted 3bits/cell MLC 2009-11; and
   2) Delayed 4bits/cell (2 companies in production) until 2012

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2009 ITRS ORTC Summary (cont.)

5) MPU GLpr – ’08-’09 2-yr flat; Low operating and standby line items track changes
6) MPU GLph – ’08-’09 2-yr flat with equiv. scaling process tradeoffs; Low operating and standby line items track changes
    1) Performance targets (speed, power) on track with tradeoffs
7) MPU Functions/Chip and Chip Size Models
    1) Utilized Design TWG Model for Chip Size and Density Model trends – tied to technology cycle timing trends and updated cell design factors
    2) High Performance MPU Transistors/chip crosses DRAM bits/chip in 2009 at 2Bt/2Gbits!
    3) ORTC line item added to deal with OverHead (OH) area model changes to deal with non-active area
8) DRAM Bits/Chip and Chip Size Model
    1) 1-yr push-out, 3yr generation “Moore’s Law” doubling cycle;
    2) smaller Chip Sizes (<60mm2) with 4f2 design factor included
9) Flash Bits/Chip and Chip Size Model
    1) 1-yr pull-in; 2yr generation “Moore’s Law” doubling cycle;
    2) growing Chip Sizes after return to 3-year technology cycle
    3) PIDS Scenario option proposal (for 2010 Update work): “mix and match” 2yr and 3yr doubling cycles across SLC and MLC products
10) New IRC 450mm Position: Pilot lines/2012; Production/2014-16
    1) New “double S-curve” graphic added to Executive Summary to clarify

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2009 ITRS Update Highlights Summary (cont.)

Some ITRS TWG Chapter Highlights (more at www.itrs.net)

- Design and System Driver Continue to Provide More Roadmap Detail and Framework for Application Needs and cross-TWG “equiv. scaling” Potential Solutions
- Litho Technology Potential Solution options Cost of Ownership Tradeoff
- PIDS tables adapted to new ORTC trends, plus Transistor “equivalent scaling” Modeling Developed for Performance and Power Options
- ERD/ERM workshops underway to prioritize “Beyond CMOS” “information processing” potential solutions, including next storage element
- A&P New Categories and TSV focus on accelerating 3D SIP and 3D Interconnect implementations
- FI – focus on productivity improvement through systematic waste reduction
- Additional Details Available in Online Roadmaps and Public Presentations at www.itrs.net ; incl. linked Future Fab 2009 ITRS special edition articles

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Backup

- ITRS online resources
- Frequency Trends
- MtM graphic
- Beyond CMOS Graphic
- Half-pitch definitions
- SICAS Technology Capacity trends

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ITRS online resources

- www.itrs.net/
  - http://www.itrs.net/Links/2009ITRS/Home2009.htm
    [2009 TRS Roadmap Publication]
  - http://www.itrs.net/Links/2009Winter/Presentations.html [2009 December Taiwan Public Conference Presentations]
  - http://future-fab.com/welcome.asp [special 2009 ITRS edition]
  - http://www.itrs.net/Links/2007ITRS/LinkedFiles/AP/AP_Paper.pdf [A&P SIP White Paper]

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New Design TWG
2007 ITRS Frequency
Historical Data vs 2005 ITRS
And Proposed* Trend Ave ~8% CAGR

Past ← → Future

2022
~14.3Ghz

10,000,000,000
9,000,000,000
8,000,000,000
7,000,000,000
6,000,000,000
5,000,000,000
4,000,000,000
3,000,000,000
2,000,000,000
1,000,000,000
0

1999 2000 2001 2002 2003 2004 2005 2006 2007

Actual
History vs ITRS
On-Chip?

~90 nm

Current ITRS model
(inaccurate)

2005/06 ITRS

~ 8%
CAGR

2007
~4.7Ghz

Actual sample of MPU
frequencies

New Design TWG
2007 ITRS Final "IS"
Ave 8% CAGR

~ 21%
CAGR

2007 - 2022 ITRS Range

* Source: Various, per ITRS Design TWG ca August 2007

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[2009 – Unchanged From 2007, 2008 ITRS]

Performance and Power Management Enabled by "Equivalent Scaling"

Design Max On-Chip Clock Frequency

Including 2005 ITRS and Final (Aug'07) 2

100.0
10.0
1.0
(Ghz)

1995 2000 2005 2010 2015 2020 2025

Year

2005/06 ITRS "WAS"

"Gap" Delayed by 3 years in 2005 ITRS

IS: Design/Architecture: reduction of maximum # 0f inverter delays to flat at 12 beginning 2007
WAS: (2001 ITRS: flat at 16 after 2006)

1.29x/year (2x/2.5yrs)

* http://en.wikipedia.org/wiki/Intel_Core_i7

1.41x/year (2x/2yrs)

*[i7/45nm/3.33GHz]… clock above those in the table are not guaranteed by Intel. Rates above 5GHz have been reported.

Core i7

3.6Ghz

Past <----> Future

PIDS/ FEP CV/I 13% CAGR? ~2x/5.5yrs

Designer power/perf. trade-off "headroom"?

New Design TWG 2007 ITRS Final "IS" Ave 8% CAGR

Design Max. Freq. 2001 ITRS

Design Max. Freq. 2003 ITRS

Extrapolation/Interpolation of 2005 WAS ITRS Proposal

Final Max On-Chip Local Clock Freq (Aug'07)

2007 Des TWG Actual History of Average On-Chip ~ 21% CAGR

2007 - 2022 ITRS Range

http://www.electronista.com/articles/10/01/20/maingear.intros.f1x.gaming.pc.series/
…Wed January 20, 2010…Custom PC maker MainGear…introduced a new series of gaming PCs….has an over-clocked Core i7 CPU to 3.6GHz,

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[2009 – Unchanged]

2007/08 ITRS "Moore's Law and More" Alternative Definition Graphic

Baseline CMOS | *Memory* | *RF* | *HV Power* | *Passives* | *Sensors, Actuators* | *Bio-chips, Fluidics*

"More Moore"

"More than Moore"

Computing & Data Storage

Sense, interact, Empower

Heterogeneous Integration

System on Chip (SOC) and System In Package (SIP)

Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

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[2009 – Unchanged]

2008 ITRS "Beyond CMOS" Definition Graphic

Baseline CMOS	Ultimately Scaled CMOS	Functionally Enhanced CMOS	Nanowire Electronics	Ferromagnetic Logic Devices	Spin Logic Devices

32nm | 22nm | 16nm | 11nm | 8nm

Multiple gate MOSFETs
Channel Replacement Materials
Low Dimensional Materials Channels

New State Variable
New Devices
New Data Representation
New Data Processing Algorithms

"More Moore"

"Beyond CMOS"

Computing and Data Storage Beyond CMOS

Source: Emerging Research Device Working Group

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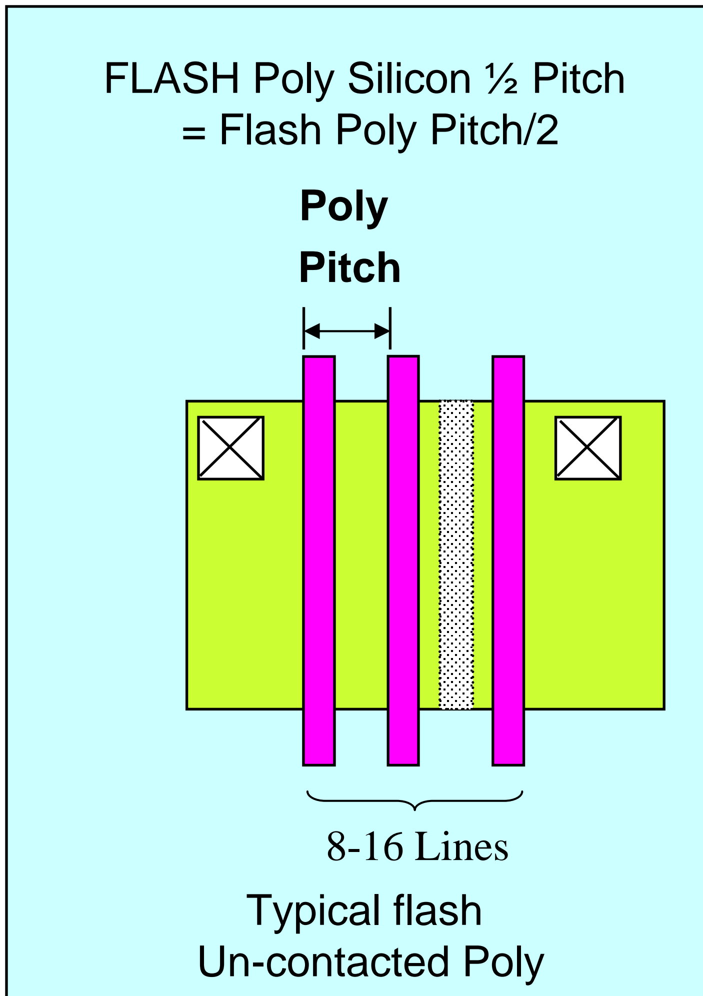
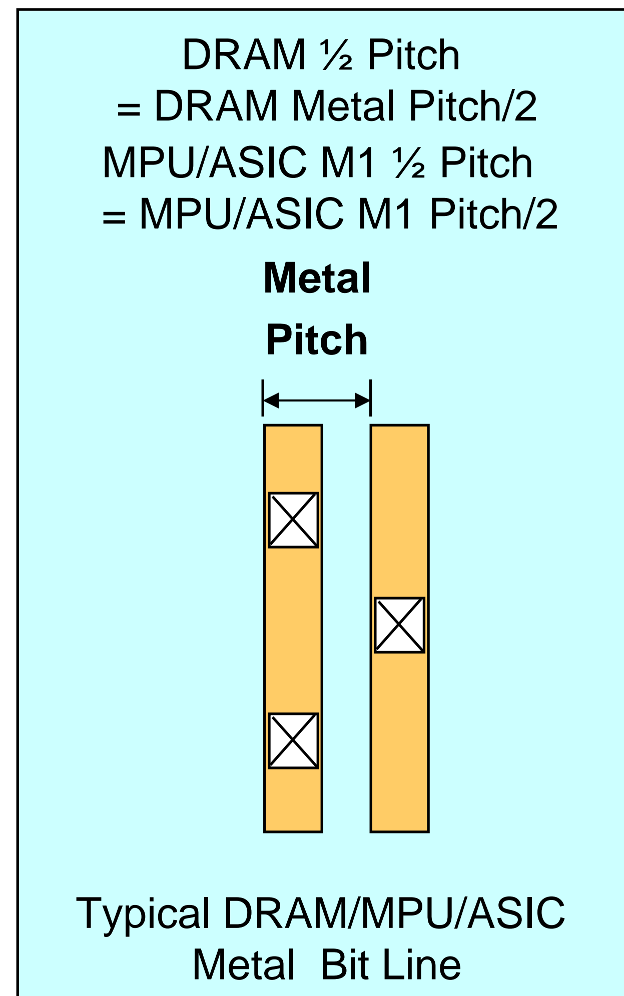
2009 Definition of the Half Pitch – unchanged

[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]





Source: 2009 ITRS - Exec. Summary Fig 1

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Updated for 2009

Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

W.P.C.=Total Worldwide Wafer Production Capacity* Sources:SICAS

Feature Size (Half Pitch) (μm)

Year: 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2013

Legend (feature size ranges): >0.7μm; 0.7-0.4μm; 0.4-0.3μm; 0.3- 0.2μm; 0.2- 0.16μm; 0.16-.12μm; 0.08-.12μm; <0.08μm

- = 2003/04 ITRS DRAM Contacted M1 Half-Pitch Actual
- = 2007/09 ITRS DRAM Contacted M1 Half-Pitch Target
- = 2009 ITRS Flash Uncontacted Poly Half Pitch Target
- = 2009 ITRS MPU/hpASIC Contacted M1 Half-Pitch Target

3-Year Cycle

2008/09 ITRS: 2.5-Year Ave Cycle for DRAM

2-Year DRAM Cycle

3-Year DRAM Cycle ; 2-year Cycle Flash and MPU

3-Year Cycle After 2010 for Flash; after 2013 For MPU

** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 2Q data for 2009. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

Source: 2009 ITRS - Executive Summary Fig 3

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