INTEL FIRST TO DEMONSTRATE WORKING 45 nm CHIPS

New Technology Will Improve Energy Efficiency and Boost Capabilities of Future Intel Platforms

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65 nm Status

- Announced shipping 65nm for revenue in Oct. 2005
- Two 65nm/300mm fabs shipping in volume (D1D and Fab 12); with two more coming in 2006
- Intel has shipped more than a million dual-core processors made on 65nm process technology
- CPU shipment cross-over from 90nm to 65nm projected for Q3/06

What are We Announcing Today?

- Intel is first to reach an important milestone in the development of 45 nm logic technology
- Fully functional 153 Mbit SRAM chips have been made with >1 billion transistors each
- The memory cell size on these SRAM chips is 0.346 μm^2, almost half the size of the 65 nm cell
- This milestone demonstrates that Intel is on track for delivery of its 45 nm logic technology in 2H 2007

45 nm Technology Benefits

Compared to today's 65 nm technology, the 45 nm technology will provide the following product benefits:

~2x improvement in transistor density, for either smaller chip size or increased transistor count

>20% improvement in transistor switching speed or >5x reduction in leakage power

>30% reduction in transistor switching power

This process technology will provide the foundation to deliver improved performance/Watt that will enhance the user experience

Intel's Logic Technology Evolution

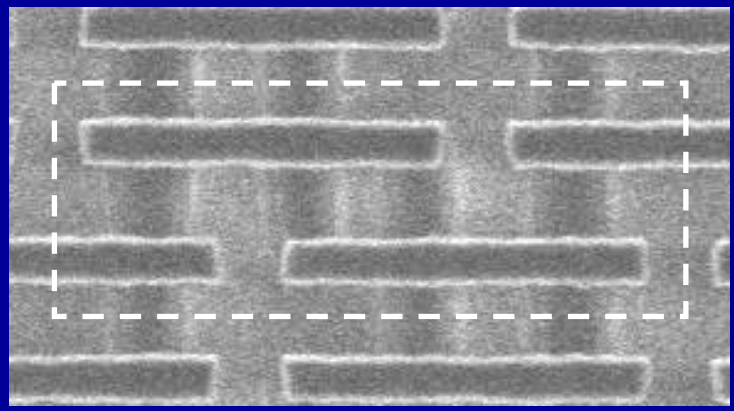
Process Name	P1262	P1264	P1266	P1268
Lithography	90 nm	65 nm	45 nm	32 nm
1st Production	2003	2005	2007	2009

Moore's Law continues!

Intel continues to develop a new technology generation every 2 years

P1266 is being developed by the Logic Technology Development group located in Hillsboro, Oregon

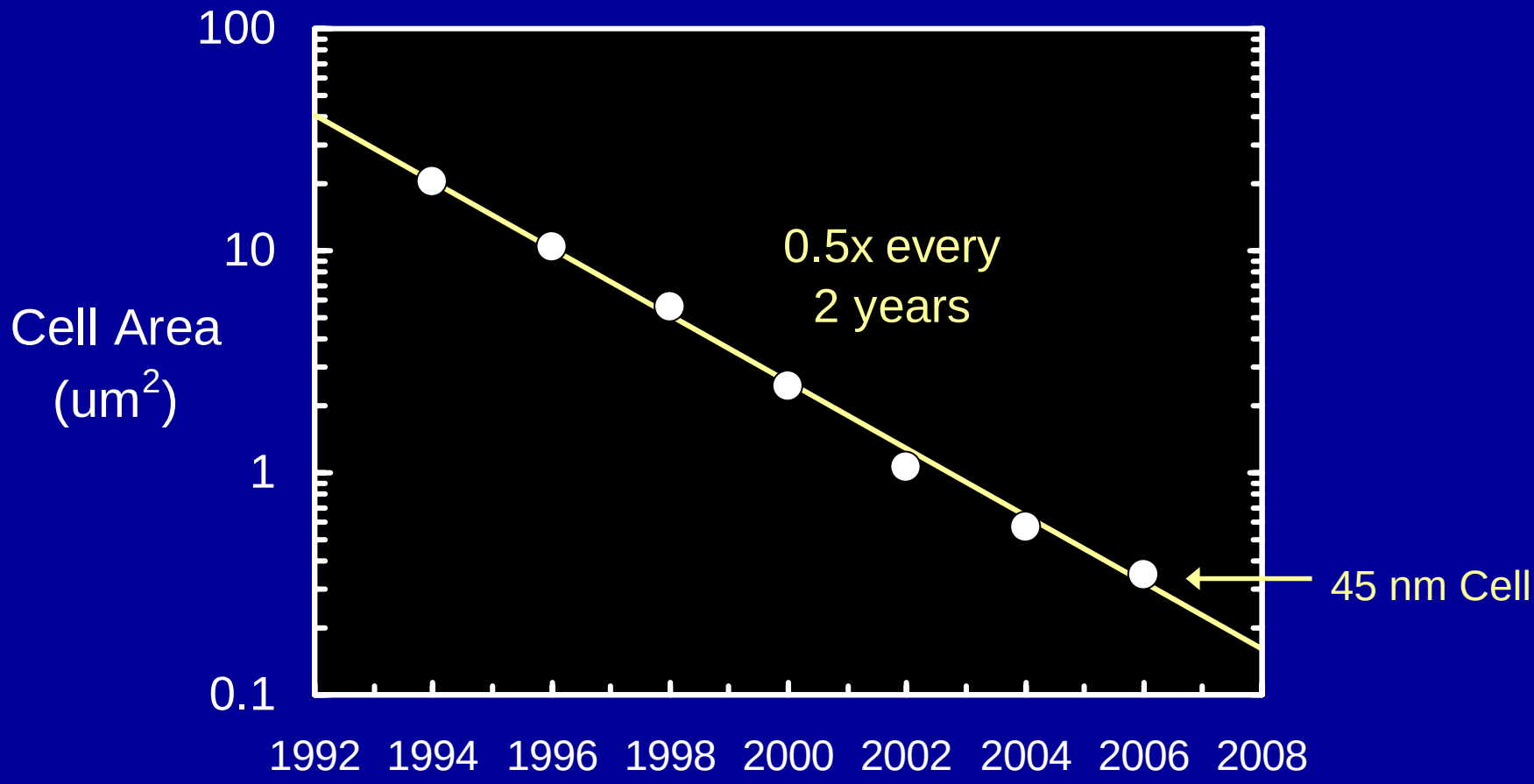
45 nm SRAM Cell



6-transistor SRAM cell area of 0.346 μm^2

193 nm dry lithography used to pattern critical layers

Intel SRAM Cell Size Trend



Transistor density continues to double every 2 years

45 nm SRAM Chip

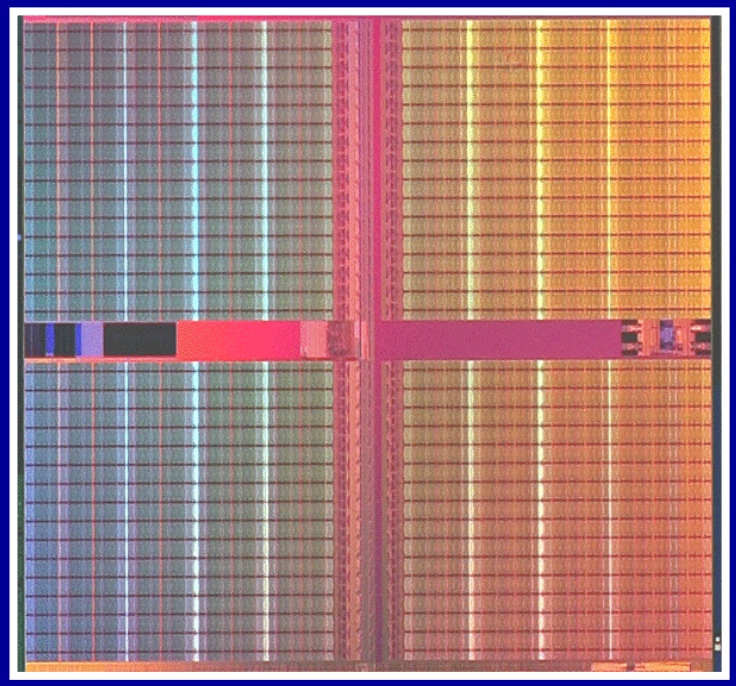
0.346 μm^2 cell

153 Mbit density

119 mm^2 chip size

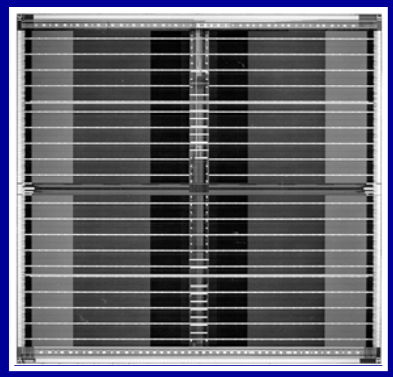
>1 billion transistors

Functional silicon in Jan ‘06



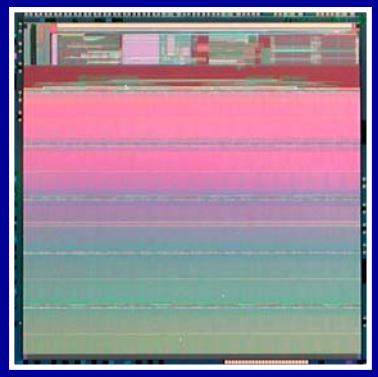
45 nm SRAM test vehicle includes all transistor and interconnect features to be used on 45 nm microprocessors

Intel SRAM Test Chips



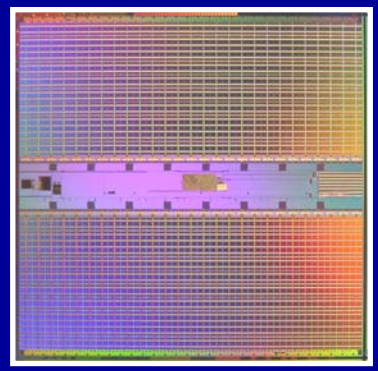
130 nm Process

2.45 μm² cell
18 Mbit
103 mm²
March ‘00



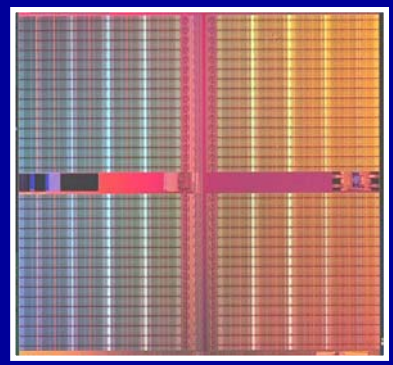
90 nm Process

1.0 μm² cell
50 Mbit
109 mm²
February ‘02



65 nm Process

0.57 μm² cell
70 Mbit
110 mm²
April ‘04

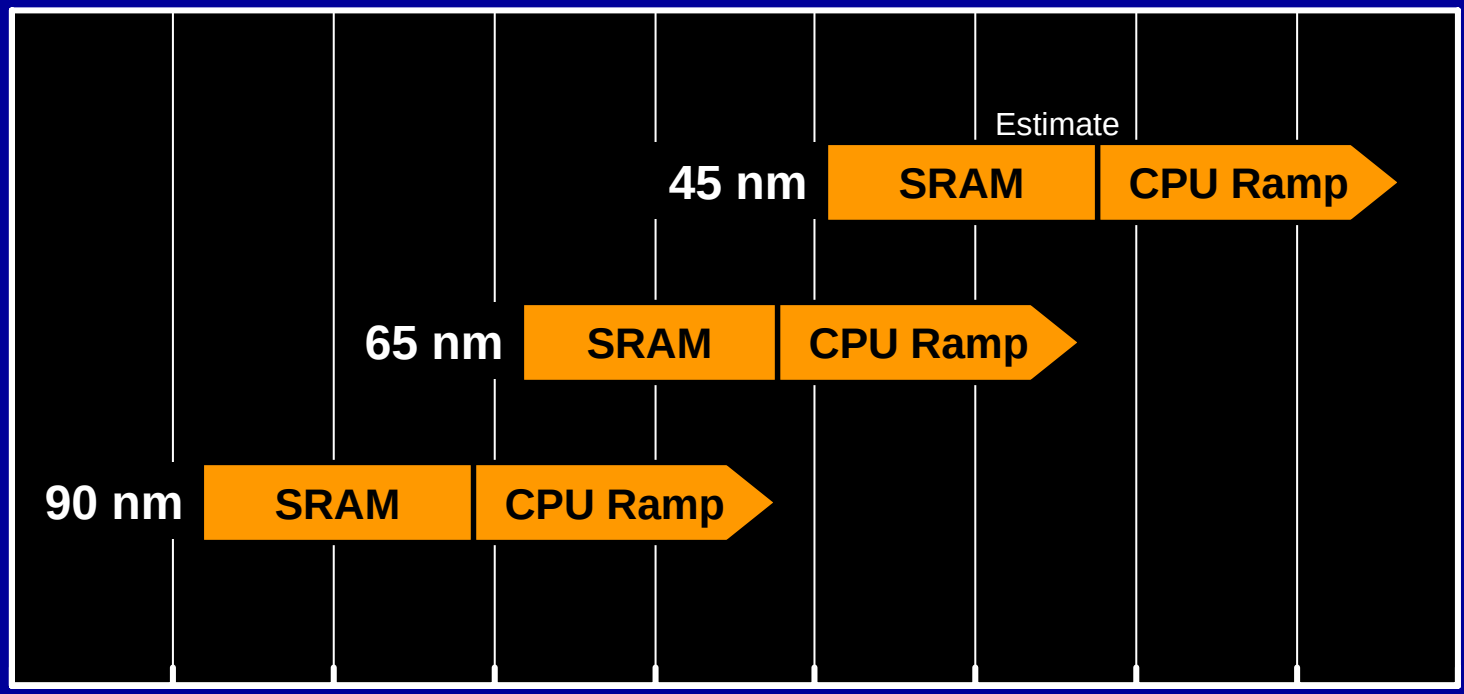


45 nm Process

0.346 μm² cell
153 Mbit
119 mm²
January ‘06

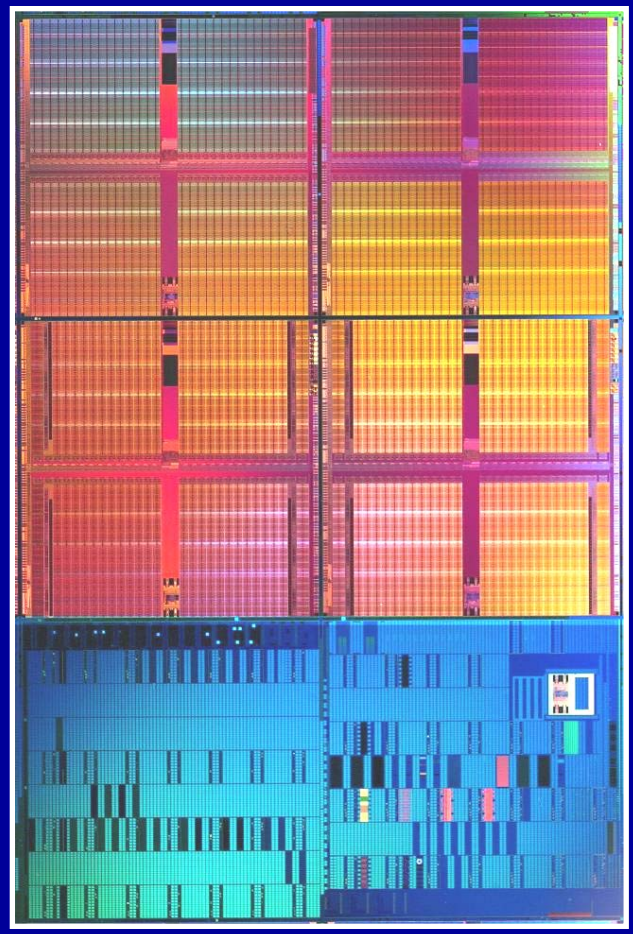
New SRAM test vehicle developed every 2 years
to lead development of logic technologies

Logic Technology Schedules



SRAM test vehicles are used to demonstrate technology performance, yield and reliability prior to CPU product ramp

45 nm Shuttle Test Chip



153M SRAM

SRAM array
PROM array
High speed register file
High speed I/O circuits
High frequency PLL/Clock

Discrete test structures

45 nm shuttle test chip includes SRAM and logic circuits for CPUs

Summary

- Intel's 45 nm logic technology is being demonstrated on fully functional 153 Mbit SRAM chips with >1 billion transistors
- These SRAM test chips exercise all of the transistor and interconnect features to be used on 45 nm microprocessors
- This 45 nm technology will provide significant density, performance and power improvements over today's 65 nm technology
- No other company has demonstrated this level of progress on its 45 nm process
- Intel's 45 nm logic technology is on track for product shipments in 2H 2007