Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 16
$3E ($5E)	Reserved									
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 17
$3C ($5C)	Reserved									
$3B ($5B)	GIMSK	INT1	INT0	–	–	–	–	–	–	page 22
$3A ($5A)	GIFR	INTF1	INTF0							page 23
$39 ($59)	TIMSK	TOIE1	OCIE1A	–	–	TICIE1	–	TOIE0	–	page 23
$38 ($58)	TIFR	TOV1	OCF1A	–	–	ICF1	–	TOV0	–	page 24
$37 ($57)	Reserved									
$36 ($56)	Reserved									
$35 ($55)	MCUCR	–	–	SE	SM	ISC11	ISC10	ISC01	ISC00	page 25
$34 ($54)	Reserved									
$33 ($53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	page 29
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								page 29
$31 ($51)	Reserved									
$30 ($50)	Reserved									
$2F ($4F)	TCCR1A	COM1A1	COM1A0	–	–	–	–	PWM11	PWM10	page 31
$2E ($4E)	TCCR1B	ICNC1	ICES1	.	–	CTC1	CS12	CS11	CS10	page 32
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								page 33
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								page 33
$2B ($4B)	OCR1AH	Timer/Counter1 – Compare Register High Byte								page 34
$2A ($4A)	OCR1AL	Timer/Counter1 – Compare Register Low Byte								page 34
$29 ($49)	Reserved									
$28 ($48)	Reserved									
$27 ($47)	Reserved									
$26 ($46)	Reserved									
$25 ($45)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								page 34
$24 ($44)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								page 34
$23 ($43)	Reserved									
$22 ($42)	Reserved									
$21 ($41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	page 37
$20 ($40)	Reserved									
$1F ($3F)	Reserved									
$1E ($3E)	EEAR	–	EEPROM Address Register							page 39
$1D ($3D)	EEDR	EEPROM Data Register								page 39
$1C ($3C)	EECR	–	–	–	–	–	EEMWE	EEWE	EERE	page 40
$1B ($3B)	Reserved									
$1A ($3A)	Reserved									
$19 ($39)	Reserved									
$18 ($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 50
$17 ($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 50
$16 ($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 50
$15 ($35)	Reserved									
$14 ($34)	Reserved									
$13 ($33)	Reserved									
$12 ($32)	PORTD	–	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 56
$11 ($31)	DDRD	–	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 56
$10 ($30)	PIND	–	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 56
...	Reserved									
$0C ($2C)	UDR	UART I/O Data Register								page 45
$0B ($2B)	USR	RXC	TXC	UDRE	FE	OR	–	–	–	page 45
$0A ($2A)	UCR	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	page 46
$09 ($29)	UBRR	UART Baud Rate Register								page 48
$08 ($28)	ACSR	ACD	–	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 48
...	Reserved									
$00 ($20)	Reserved									

Notes: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. Some of the Status Flags are cleared by writing a logical “1” to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a “1” back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.