A arquitetura Cell

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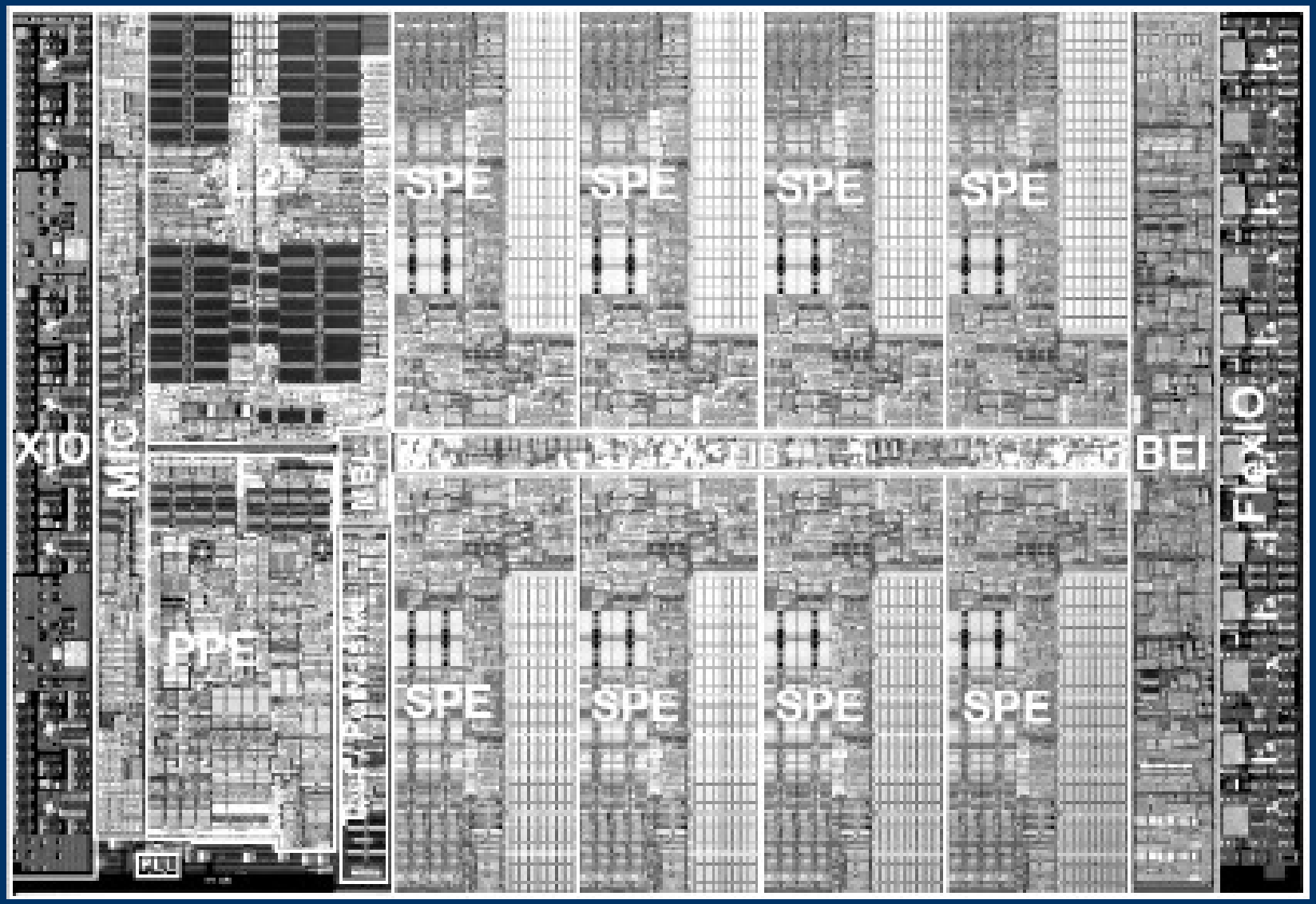
Organização

- Power Processor Element (PPE)
  - Processador principal baseado na arquitetura POWER
  - Controlador das SPEs
  - Cache L2
- Synergistic Processing Elements (SPE)
  - Responsável por tratar workload
  - Possui uma Local Store, ao invés de cache.
- Element Interconnect Bus (EIB)
  - Conecta PPE + SPE + I/O
  - I/O: 2 interfaces Rambus independentes

Die do Cell



Comparativo Cell x Emotion Engine

	Sony Emotion Engine	Cell Processor
CPU Core ISA	MIP64	64-bit Power Architecture
Core Issue Rate	Dual	Dual
Core Frequency	300MHz	~4GHz (est.)
Core Pipeline	6 stages	21 stages
Core L1 Cache	16KB I-Cache + 8KB D-Cache	32KB I-Cache + 32KB D-Cache
Core Additional Memory	16KB scratch	512KB L2
Vector Units	2	8
Vector Registers (#, width)	32, 128-bit + 16, 16-bit	128, 128-bit
Vector Local Memory	4K/16KB I-Cache + 4K/16KB D-Cache	256KB unified
Memory Bandwidth	3.2GB/s peak	25.6GB/s peak (est.)
Total Chip Peak FLOPS	6.2GFLOPS	256GFLOPS
Transistor Count	10.5 million	235 million
Power	15W @ 1.8V	~80W (est.)
Die Size	240mm^2	235mm^2
Process	250nm, 4LM	90nm, 8LM + LI