

McPAT

Multicore Power, Area, and Timing

MO801

Power Consumption Basics

- Dynamic Power
 - Every time a bit flips, power is consumed
 - Real work being done → power dissipation
- Static Power
 - Also known as leakage power
 - Power consumed by active devices
 - Idle device → power dissipation
- Short-circuit Power
 - Power consumed during the small period of time

ITRS

- International Technology Roadmap for Semiconductors
- The last version is the 2013 ITRS
- Provides expected evolution path for several technologies and processes
- <http://www.itrs.net>
- If you want to scale your results to the future, look at some of the ITRS documents

Other Tools

- CACTI for memory hierarchy
 - First tool in rapid power, area and timing estimation
- Wattch for processor power estimation
 - Enabling a tremendous surge in power-related research
- Orion for Network on Chip estimation
 - Combined Wattch's core power model with a router power model

Problems with other tools

- CACTI
 - No integration with other tools
- Wattch
 - No timing and area models
 - Only models dynamic power consumption
 - Use simple linear scaling model
- Orion2
 - No short circuit power or timing
 - Incomplete

Integrated Approach

- Power
 - Dynamic → Similar to Wattch
 - Short Circuit → IEEE TCAD'00
 - Leakage → Mastar & Intel
- Timing
 - CACTI with extension
- Area
 - CACTI
 - Empiric modeling for complex logic

Processor Characteristics

- In-order and Out-of-order
- Single and Multi-threaded
- Low Power
- Shared/coherent caches
 - With directories
- Network on chip (NoC)
- On-chip memory controller
- On-chip I/O controllers

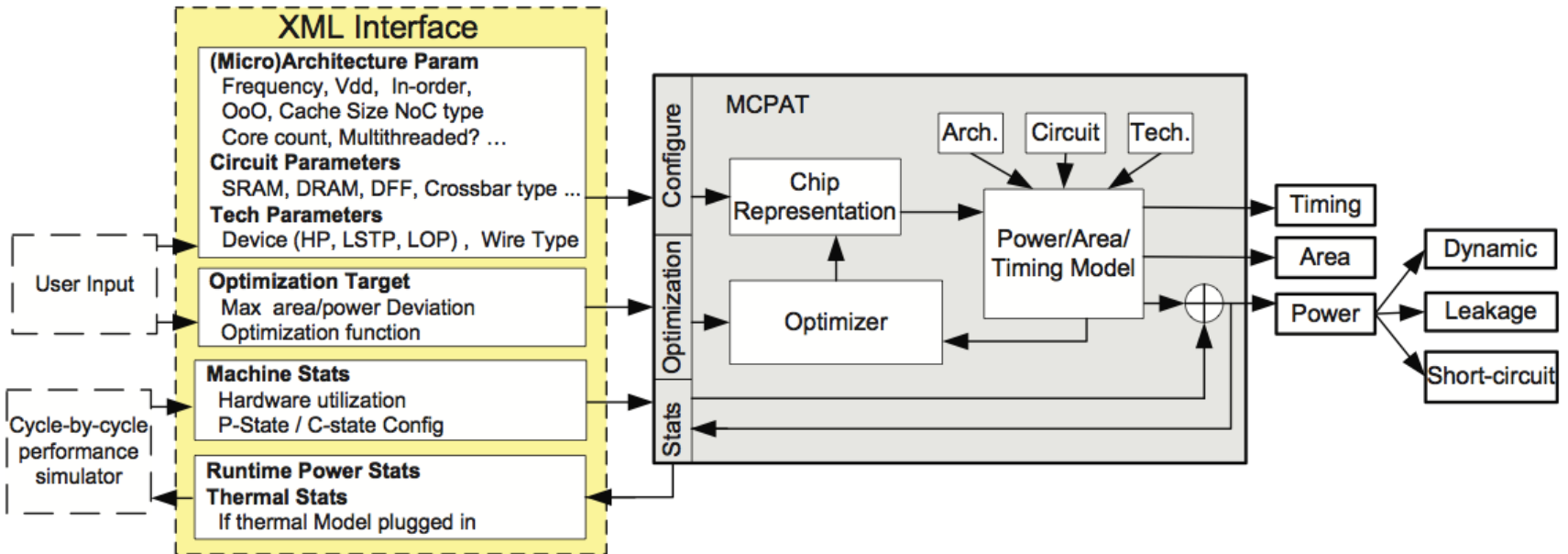
Baseline Models

- In-order models are based on Sun Niagara family
- Out-of-order models are based on:
 - Intel P6 for reservation station
 - Intel Netburst and Alpha 21264 for physical register file
- Low power embedded processor are based on ARM Cortex A9

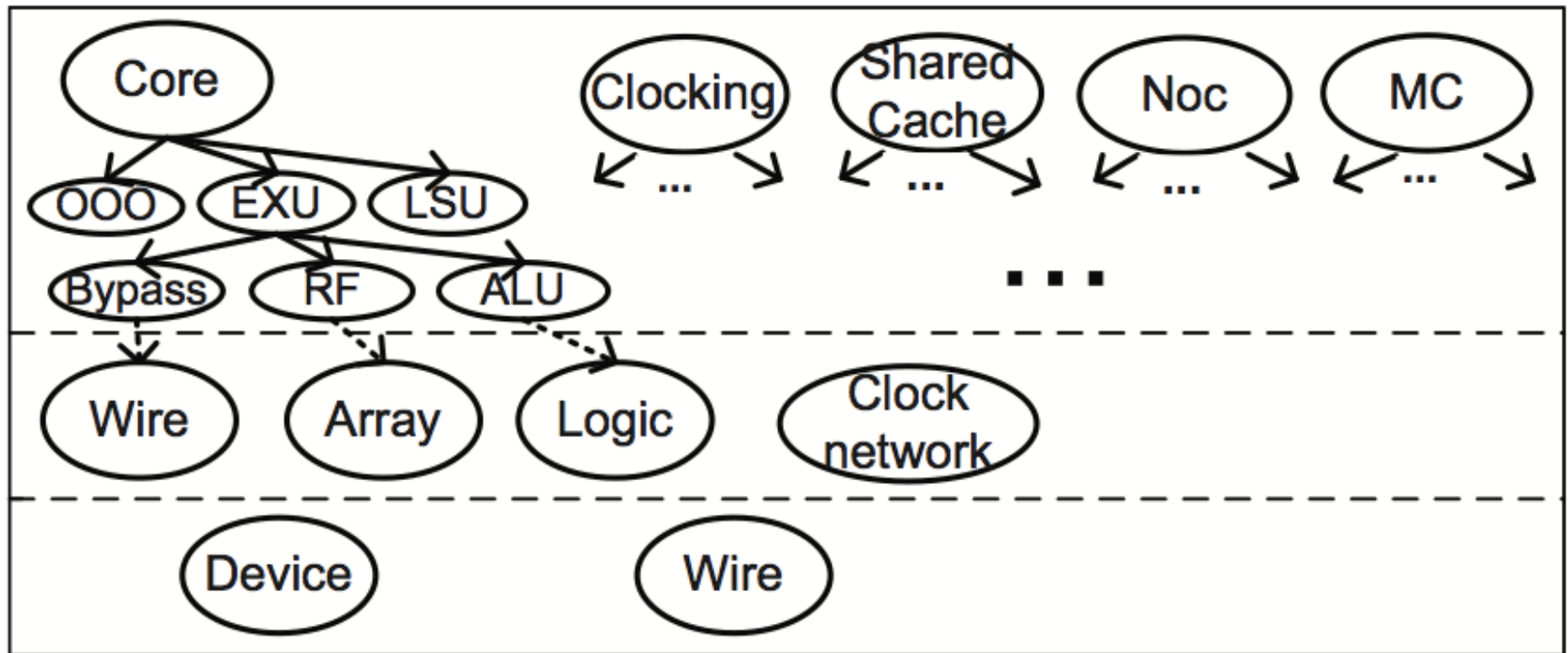
Technology Processes

- Used ITRS values for
 - 90nm, 65nm, 45nm, 32nm, and 22nm
- Distinct types of transistor specific for each technology according to ITRS
- Support for DVS
- Extensive search to find optimal designs that satisfy the target clock frequency
- Timing constraint include both throughput and latency

Block diagram



Hierarchy Modeling



Architecture Level

- Core
 - Divided into several main units: IFU, EXU, LSU, OOO issue/dispatch
- NoC
 - Signal links
 - Routers
- On-Chip Caches
 - Coherent cache
- Memory controller
 - 3 main hardware structure
 - Empirical model for physical interface
- Clocking
 - PLL and clock distribution network
 - Empirical model for PLL power

Circuit Level

- Wires
 - Short wires as one-section Pi-RC model
 - Long wires as a buffered wire model
- Arrays
 - Based on CACTI with extensions
- Logic
 - Highly regular → CACTI
 - Less regular → Model from Intel, AMD, and SUN
 - Highly customized → Empirical, from Intel and Sun
- Clock Distribution Network
 - Separate circuit model
 - Global, domain, and local

Second Project

- Select a one machine
- Select one program from PARSEC
- Measure one program execution time and energy consumption
- Use McPAT to find a better hardware configuration to execute this same program
- You will need to consider OOO and Cache configurations
- Recommended tools
 - McPAT, dinero, PIN, PARSEC