

Final Project Presentations — Part 2

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Goal of this class

Module 6, Class 3: remaining pairs present. **Project 3 due at end of this class.**

At the end of this class, you should be able to:

- Deliver a complete 15-minute presentation with live demo or recorded video of your accelerator.
- Explain your roofline analysis and what it reveals about your design's efficiency ceiling.
- Reflect critically on the design decisions you would change with hindsight.
- Evaluate peer presentations through focused technical questions during Q&A.

Format (same as Part 1)

- 15 minutes + 5 minutes Q&A per pair.
- Live demo on Tang Nano 9K or recorded video.
- Same grading criteria as Part 1 (see M06A02).

Presentation schedule

(Filled in at the start of class)

Slot	Pair	Project title
1		
2		
3		
4		
5		

Project 3 submission checklist

Submit via the course platform by the end of this class:

- [] `src/` — all SystemVerilog source files (accelerator + integration changes).
- [] `tb/` — Verilator testbench(es): unit test for accelerator, integration test.
- [] `sw/` — C driver (`accel_driver.c/h`) and modified `kws_kernel.c`.
- [] `results/profiling_baseline.txt` — M04A03 profiling output (cycles per layer, software).
- [] `results/profiling_accelerated.txt` — M05A03 profiling output (cycles per layer, with accelerator).
- [] `results/utilization.txt` — nextpnr resource report (`make load` output).
- [] `results/roofline.md` — arithmetic intensity calculation, roofline position, bound identification.
- [] `README.md` — design decisions, build instructions, known limitations.

Class discussion: comparing designs

After all presentations, a 15-minute open discussion:

- Which design achieved the highest system speedup? Why?
- Which roofline analysis was most insightful?
- Did anyone find a bug in the profiling stage that changed their design decision?
- What would the class do differently if starting over?

Next class

Retrospective — the full abstraction stack from gates to AI inference, what comes next, and course feedback.